1106 C
TECHNICAL
MANUAL

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CORE STORAGE EXPANSION

FOR THE 1130 SYSTEM

Accelerator 1131

COMPUTER HARDWARE INC.
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CHI 1106/C

TECHNICAL MANUAL

CORE STORAGE EXPANSION

FOR THE 1130 SYSTEM

WARRANTY

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COMPUTER HARDWARE INC'S obligation under this warranty is limited to servicing or adjustment of any equipment returned to the factory up to one (1) year from date of delivery. If the failure has been caused by misuse, operation in excess of specification guarantees, or modification by the customer, repairs will be billed at cost. In such cases, a cost estimate will be submitted before work is started.

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SECTION 1 - GENERAL DESCRIPTION

Features

The CHI 1106/C core memory system provides expanded storage for the IBM 1130 system. It is a 3D, 3-wire memory system that is available in increments of 8K to a maximum of 65K (65,535 words). CHI core may be used alone or in conjunction with CPU storage. Modular construction permits customer maintenance and field installation of additional storage.

An access time of 250 nanoseconds permits operation with both 2.2- and 3.6-microsecond processors. If necessary, timing components can be changed in the field.

The 1106/C is packaged in a 24-inch wide enclosure coordinated with the 1131 CPU; the sloping writing top, pencil strip and other features are continued by the 1106/C design.

Equipment Arrangement

CHI CORE is interfaced to the host system through slip-on connectors attached to the pin side of the IBM logic gates; no permanent connections or circuit alterations are made. Because all connectors are mechanically attached they can be easily removed to isolate CHI CORE from the host system.

A box containing a circuit board is mounted inside the host system with hook and loop adhesive pads. The purpose of this board is to convert the IBM signals to integrated-circuit voltage levels and to repower the converted signals

back into the computer. (The interface circuits require a negligible amount of power from the IBM computer. This has been done to insure that the IBM circuits which are involved will not be subject to any stress which might cause them to fail).

The CHI CORE cabinet contains the core storage power supplies, addressing circuitry, and core modules. Circuits are provided to shut off the power supplies should voltages develop that could cause component failure or marginal operation.

Back-up Electronics

This option provides the customer with a means of repairing his own equipment. It consists of a duplicate set of electronics, including an 8K block of memory, which can be easily interchanged with the primary system. This backup system guarantees the user that, in the event of a failure, down time will be minimal while maintenance cost is greatly reduced. No special equipment is required to use the backup system.

Power

The CHI CORE operates on a 115 VAC power source which must have the same ground as the host system.

The CHI CORE power system is ordinarily turned on and off by sensing the status of the host system's +6 voltage supply. This function can be bypassed via a manual switch at the back of the CHI CORE cabinet.

System Integration

Systems with total core storage (CHI CORE or CPU + CHI CORE) up to 32K function identically to IBM-supplied storage of equivalent size. However, programming techniques are often used that will prevent operation of existing software on systems of greater than 32K. An example is the standard IBM 1130 Monitor program.

The Company should be contacted for information concerning software modifications and other considerations when 40K or larger installation is being planned.

SECTION 2 - INSTALLATION INSTRUCTIONS

Preliminary

1. Remove all packing materials except the plastic sleeve covering the control board connector on the signal cable.
2. Compare the contents of the shipment with the packing list and check for damage. Report any damage to the freight carrier and to Computer Hardware.
3. Power down the 1130 system. Open the 1131 front door, loosen the inner door screw, open the inner door and operate the circuit breaker to OFF.
4. Remove the 1131 typer paper stand, open the 1131 rear doors and top cover and swing out both A and B gates as a unit.
5. Clean (Use items 1 & 2 on List of Materials, Figure 5) the hinge ends of the gates where adhesive devices are to be mounted (See Figure 1, Key Numbers 1,2,3).

Receiver-driver Box (RDB)

1. Peel the backing from the four loop strips which are attached to the hook strips on the rear of the box. Align the box with the gate hinge and press the box in place. Slowly pull off the box and rub the loop strips to ensure a good bond.

2. Remove the RDB front cover and check the following:
   A. Proper timing capacitor installed (Figure 11, Note 1).
   B. Correct select plug installed in IC socket 2 (Figure 2).
3. Remount the RDB.

CPU Cable

1. Along the top of the B gate circuit boards, clean (use Items 1 & 2) the underside of the silver-colored steel angles around the following points: 8, 15 and 18½ inches from the hinge end of the gate. Install three cable mounts (Item 4) at those points with the nylon loops parallel to the gate.
2. Connect the CPU interface cable to J5 and J6 of the RDB and route the wrapped portion over the top of the gate end plate (Figure 1, Key 4). Gently push the paddle cards onto the groups of pins specified by the paddle card labels (ref. IBM 1131 Manual Vol. 001, AE000).

Note 1. During the installation of the CPU cable all IBM pins to be used must be cleaned (use Items 1 & 5).

Note 2. When installing the paddle cards, care must be taken to insure that the wire-wrapped portion of the IBM pins do not enter the connector and distort the contact fingers. Such damage will cause intermittent or no

connection. Should this happen, Figure 4 describes a tool which can be used to restore the contact fingers to their original positions.

3. Secure the CPU cable to the mounts installed in step 1 with three small cableties (Item 6).

4. Attach the single wires from the paddle cards to the CPU points as labeled. The unlabeled eight-inch wire from C1-T4 is connected as follows:

TYPE 1131	1131 MODELS	CONNECT TO
All 2.2 usec	3B, 3C, 3D	C1-H3-D13
3.6 usec with B-gate storage	1A, 1B, 2A, 2B	C1-N2-D02
3.6 usec with D-gate storage	2C, 2D	C1-D2-B04

Apply label (Item 7) by cutting out and folding over wire between signal name and pin number.

5. In accordance with system configuration, make the following connections (Items 9, 10) except use Item 12 (Wire Wrap) for "Model 4" connections and install the appropriate labels (Items 7,8):

1130 SYSTEM	CONNECT FROM	TO	LABEL TITLE	LABEL LOCATION
A11	---	---	"READY"	Over CE lamp 1
4K 1131 without address bit 1 lamps installed	---	---	"IAR 1"	Over CE lamp 4
	---	---	"SAR 1"	Over CE lamp 5
	B1-B3-D04	A1-A4-D12	"I BIT 1," "CE 4"	On jumper
	B1-B2-B07	A1-A4-B13	"M BIT 1," "CE 5"	On jumper
More than 32K total storage	---	---	"IAR 0" "SAR 0"	Over CE lamp 2 Over CE lamp 3
	B1-B3-D05	A1-A3-D13	"I BIT 0," "CE 2"	On jumper
	A1-T1+8"	A1-A4-B12*	---	---
1131 with 3.6 usec D-gate storage	C1-D2-D12	C1-D2-B03	"DRIVER OUTPUT" "3.6 D GT "INHIBIT	On jumper
Model 4	A1-B1-E11 A1-B1-B09 A1-B1-D09	A1-F1-E11 A1-F7-B10 A1-F7-D04		

*If not used, tie to cable bundle with small cabletie and apply "NOT USED" label.

1106 Signal Cable

1. Install two cable mounts on the face of the gate hinge plate (Figure 1, Key 2,3).
2. Verify that the cable hanger clamp is positioned 26 inches from J4 of the signal cable.
3. Connect J4 of the signal cable to the RDB at the bottom. With a large cabletie (Item 9), securely fasten the cable to the mounting pad (Figure 1, Key 2). Connect the shield lead to the cable clamp mounting screw below pin group A1-A8.
4. Pass the covered (J3) end of the signal cable over the typer cable (See Step 9 if this is not clear), down the hinge tube, over the cables at the base of the tube and out through the cable exit hole.
5. Form the signal cable in an S-shaped bend so that it meets the hinge tube just below the file bracket. Tie it to the front surface of the tube with a large cabletie, (Figure 1, Key 5) leaving the ties loose enough for adjustment. Dress the cable down the front of the tube and apply a second tie.
6. The hanger clamp on the signal cable should now be in line with the cable pin in the next hole. If it is not, redress the cable, or if more than a half an inch off, loosen and reposition the clamp. When properly positioned, the cable can be pulled toward the rear of the 1131 until the clamp hits the edge of the exit hole, yet there will be no strain on the lower cabletie. Replace the cable pin, being sure to retain all existing system cables.

7. Tighten the cableties and cut off the excess. The cable must be held against the front surface of the tube tightly enough to prevent any twisting motion from occurring.
8. Leaving a loop (1/2 inch larger than cable), loosely attach the signal cable to the mounting pad between the gate hinge screws (Figure 1, Key 3) using a large cabletie. (The loop is necessary to allow the cable to move out of the way when the two gates are spread apart for servicing).
9. Slowly close both gates while looking from the top and rear for interference with 1131 parts. Be especially careful of the IBM paddle cards inserted into jacks PF1-PF9, located just below the RDB (gate closed). The upper bend in the signal cable should fit inside the file bracket and to the left of the typer cable. (If the signal cable were to the right, it would press the typer cable against the file bracket edge). Also make sure the IBM wires from TB-5 are not trapped between the A1-T1 paddle card and the frame when the gate is closed. If necessary dress the wires closer to TB-5.

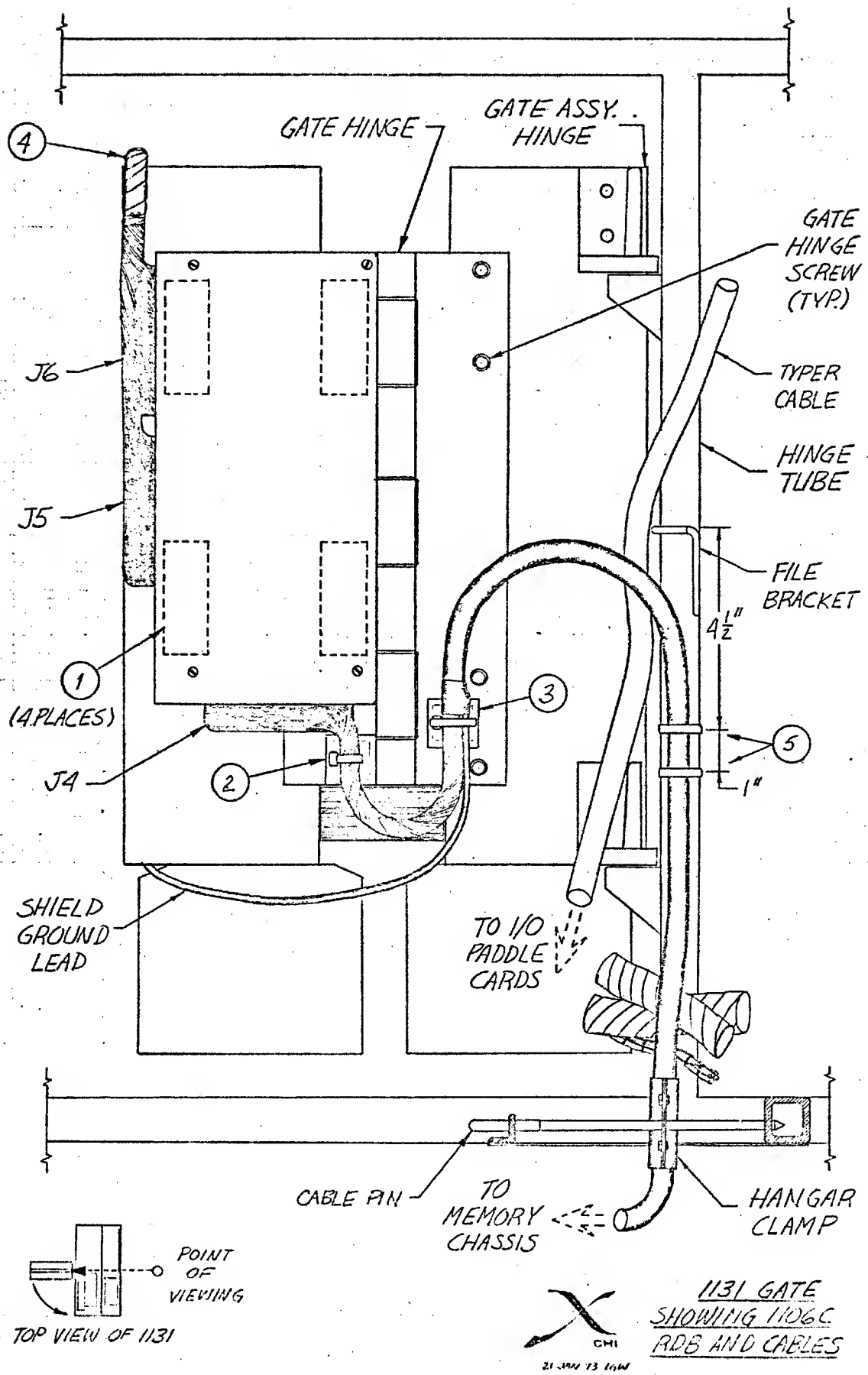
Memory Chassis

1. Remove the card bay access covers and memory control board (MCB). Check the MCB for correct select plugs (Figure 2).
2. Replace the MCB. Verify that core modules are installed per system requirements (Figure 3).

3. Install power cord in the receptical at the rear of the chassis and connect to 115VAC. Using voltage and then resistance checks, verify that the 1106 and 1131 have a common cabinet ground. Disconnect the power cord.
4. Connect the free end of the signal cable to J3 on the edge of the MCB. Fasten the cable to the side of the chassis with the clamp and screws provided. The shield lead is attached to one of the clamp screws.
5. Reconnect the power cord.

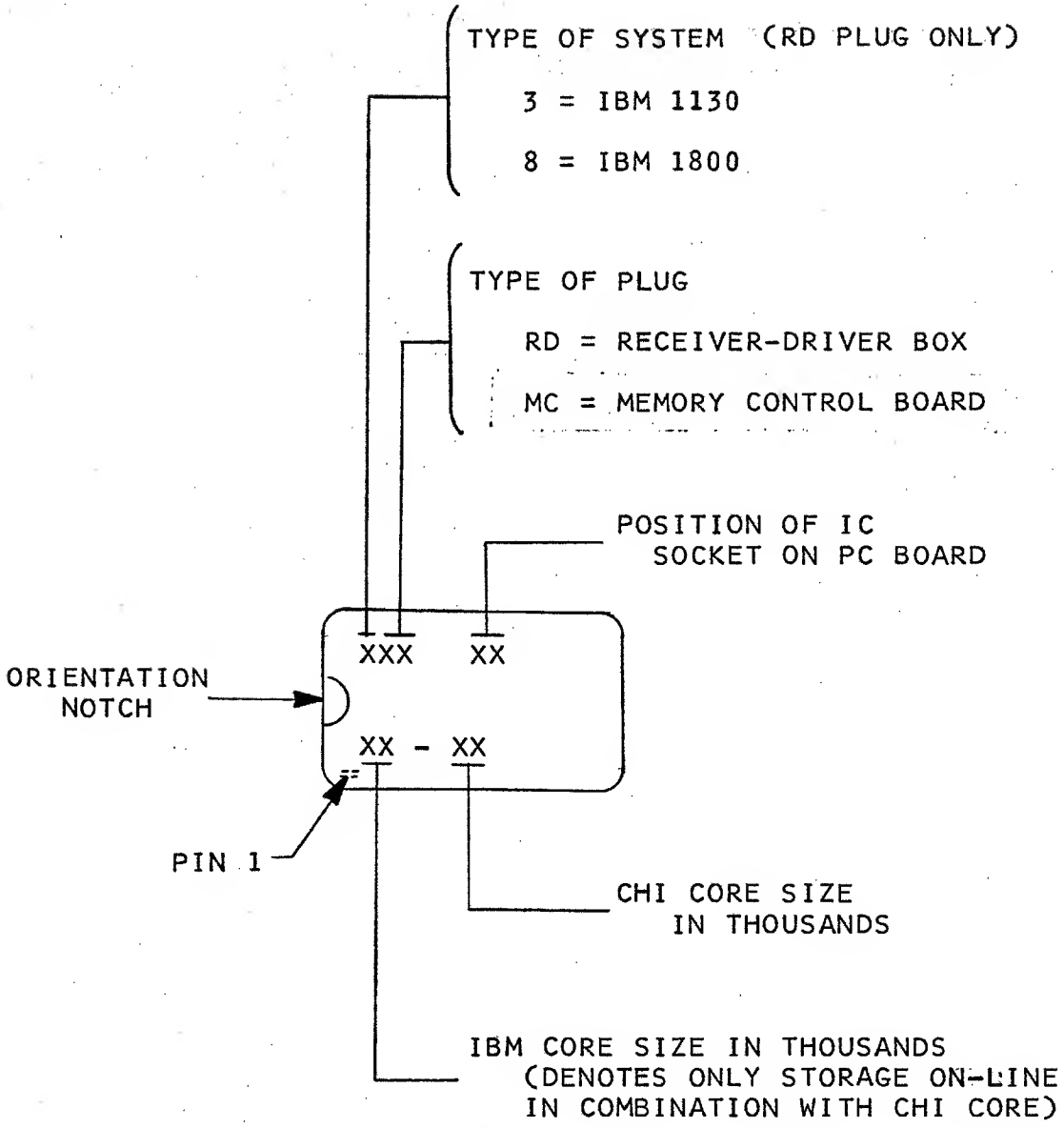
Final

1. Restore the 1131 circuit breaker, operate the 1106 POWER switch to REMOTE and operate the 1131 POWER switch to ON. (Refer to Sec. 3 of the manual for control and indicator functions). If the READY light is on, begin operational tests. (See Appendix A for programs that may be used to verify correct operation or aid in debugging).
2. Lower the four glides on the bottom of the cabinet until they nearly touch the floor.
3. Remove four 6-32 screws from the sides of the cabinet frame bottom. Fit the U-shaped skirt (kick plate) around the frame bottom (open side to the rear). Reinstall the four 6-32 screws. Snap side, front and rear panels in place, and position the cabinet in it's permanent position. If the customer desires, lower all four glides to raise the casters off the floor and to line up the cabinet top with that of the 1131.



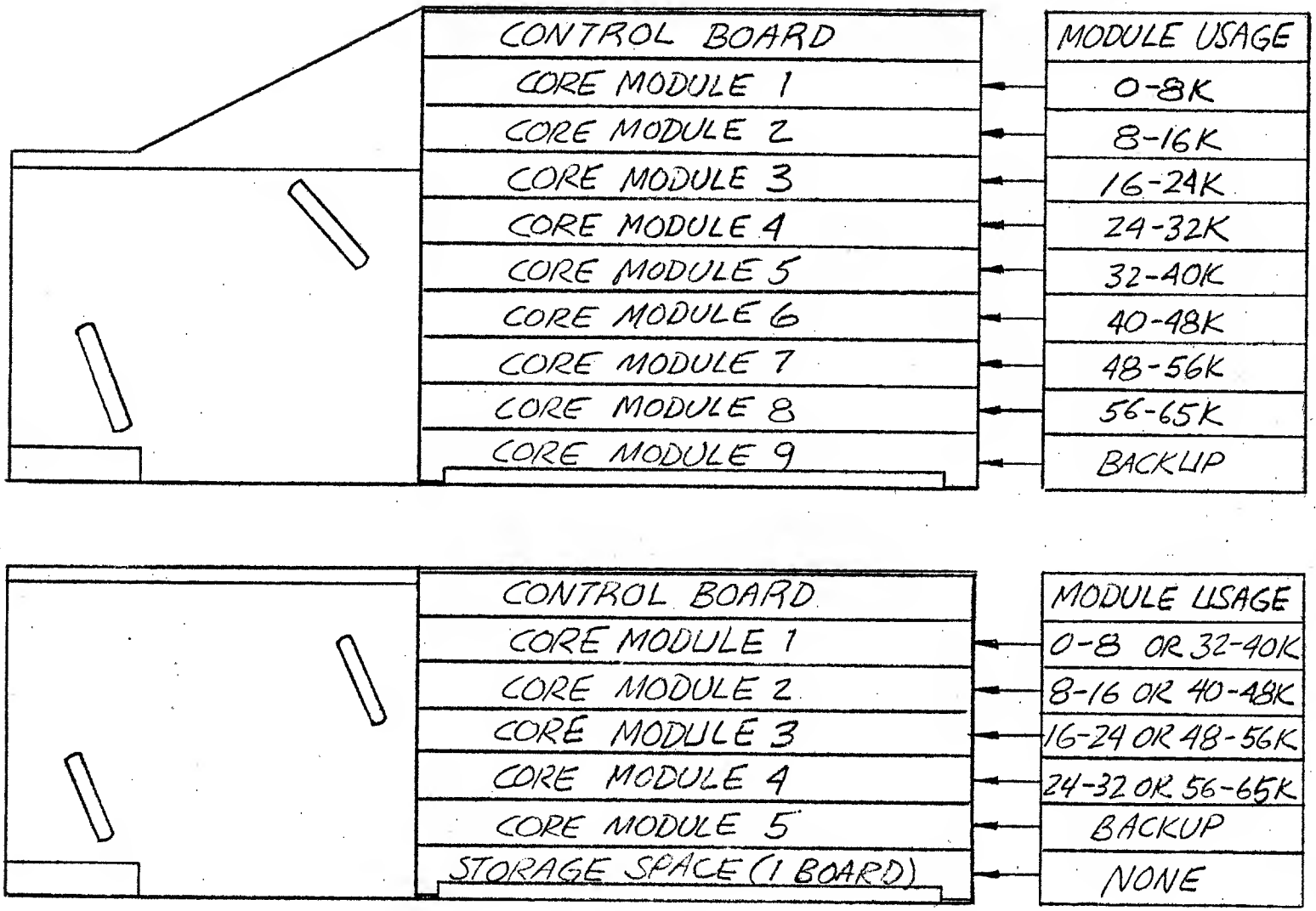
1131 GATE SHOWING 1106C RDB AND CABLES

FIGURE 1



SELECT PLUG IDENTIFICATION

FIGURE 2

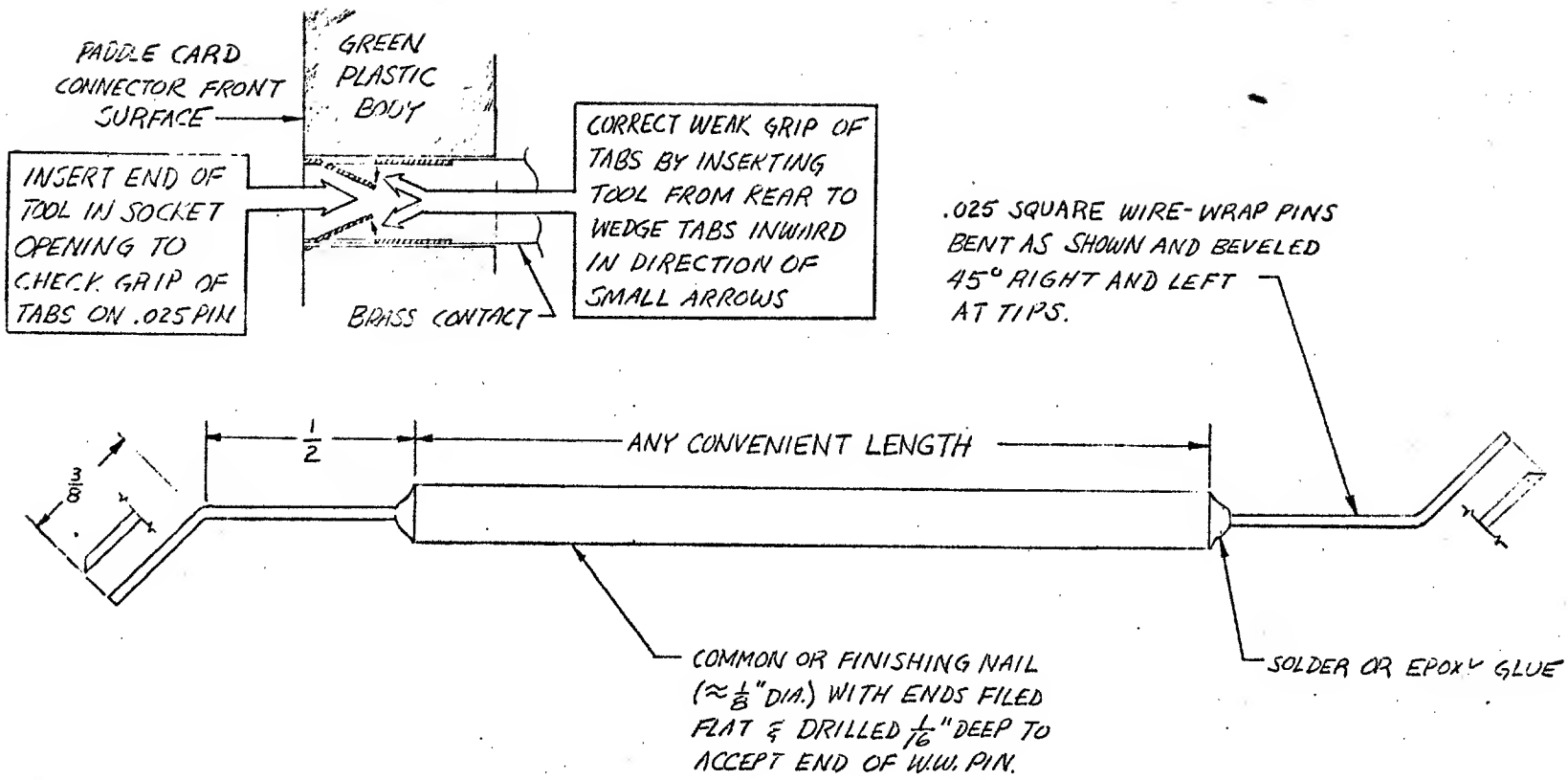


MEMORY CHASSIS CIRCUIT BOARD LOCATIONS

CHI

19 JAN 73 LGW

FIGURE 3



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PADDLE CARD CONNECTOR TOOL & METHOD OF USE

FIGURE 4

QUAN	CHI FILE	DESCRIPTION	MFGR.	PART NO.	ITEM
AR	NOT SUPPLIED	ALCOHOL, ISOPROPYL, 91%	LILLIE	M-19	1
AR	NOT SUPPLIED	WIPERS, CLEANING	KIMBERLY-CLARK	900S	2
					3
5	210377	MOUNT, CABLE, ADHESIVE BACKED	PANDUIT	ABMS-A	4
AR	NOT SUPPLIED	SWABS, COTTON	JOHNSON & JOHNSON	8762BH	5
3	211094	CABLETIE, .62 ID MAX, S-L	THOMAS & BETTS	TY-23M	6
1	211917	LABEL SET, INSTL., 1106/1130 GENRL	CHI	DB-1122-4	7
1	211918	LABEL SET, INSTL., 1106/1130 4K CPU	CHI	DB-1122-6	8
4	211101	CABLETIE, 1.75 ID MAX, S-L	THOMAS & BETTS	TY-25M	9
1	211901	JUMPER-.025 SQ PIN, 2 INCH	CHI	CB-1259-1	10
3	211906	JUMPER-.025 SQ PIN, 12 INCH	CHI	CB-1259-11	11
3 FT	211493	WIRE, 30 AWG SOLID, KYNAR INSUL.	CHI	DD-1002-59	12

LIST OF MATERIALS FOR
1106C/1130 INSTALLATION

FIGURE 5

SECTION 3 - OPERATION

Power Controls (1106 Rear Panel)

Figure 6 illustrates the power controls and explains their functions.

False Power Faults

The voltage monitor board may interpret quick on/off cycling of the power switch as a power fault. While harmless, a false power fault requires further action to restore operation. To avoid this, wait thirty seconds before powering up the system after shut-down.

Fuses

The primary fuse (3-amp fast blow) is located in the holder adjacent to the power cord receptacle. Secondary fuses are mounted within the chassis. A blown fuse is indicative of trouble requiring the attention of service personnel. Replacement of fuses without investigation of the cause is not recommended and may lead to further damage.

Power Indicator (CPU Display Panel)

The operator can determine system readiness by observing CE lamp 1, labeled "READY". This lamp provides the same indication as does the READY lamp on the 1106 chassis. Further, as it

is associated with the receiver-driver box in the 1131, its operation provides proof that all cables are connected and that power is being supplied to the most distant circuits.

Data Indicators (CPU Display Panel)

Systems having greater than 32K utilize address bit 0 for which there is no display provided on the 1131. To provide this information, CE lamps 2 and 3 are labeled "IAR 0" and "SAR 0", respectively.

Some 4K systems are also lacking bit 1 lamps. In such cases, CE lamps 4 and 5 are used for this purpose.

It should be noted that the SAR display shows only the addresses generated by the CPU, and not those from peripheral devices.

Bit 0 (or 1) Disable Switch (optional)

This switch is located on the top of the receiver-driver box so that it is accessable when the 1131 top cover is raised. It reconfigures a combined 1131/1106 storage of "non-standard" size to one of 16 or 32K. This allows running IBM diagnostics in the largest amount of core possible.

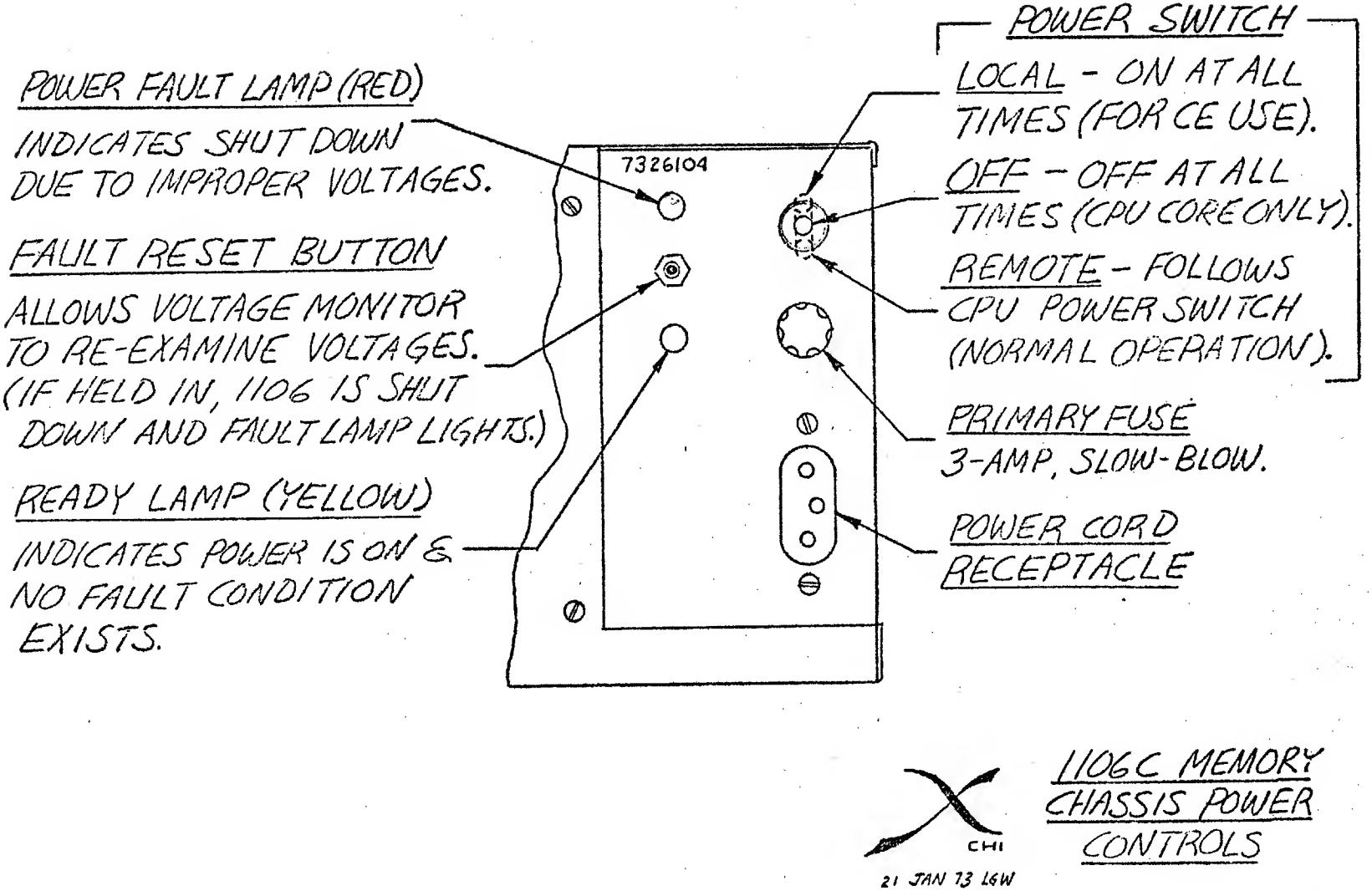
Spare Module Switches (optional)

On models with a spare core module ("backup electronics"), a bracket containing 4 toggle switches, S1 through S4, is mounted on the printed circuit (mother board) containing the core module

receptacles. Throwing a switch to the right will disable the module in the corresponding position and substitute the spare. If more than one switch is thrown at one time, the modules corresponding to the higher switches will simply not function, and parity errors will result. To prevent errors, the CPU must be in the stopped condition (RUN light out) when the spare is switched in.

Disabling CHI Core

When desired by IBM service personnel, the 1106 may be disabled by operating the power switch to OFF. This effectively isolates the 1106 circuits and the CPU storage functions in the normal manner.



1106C MEMORY CHASSIS POWER CONTROLS

FIGURE 6

SECTION 4 - PREVENTIVE MAINTENANCE

Cooling Fan Filter

At least once each month, remove the cabinet side panel and check the condition of the fan filter screen. If an appreciable amount of dust has collected, cooling will be impaired.

Four slots are provided in the filter frame edge to allow the use of a screwdriver in the event the frame cannot be pulled off by hand. Running hot water is usually all that is necessary to clean the filter. When replacing the inner screen, the dimples in the screen must fit over the fan mounting screws.

Cabinet Exterior

A wax-type cleaner, e.g. Johnson's Jubilee, is recommended for the writing surface. If liquids are used, take care to prevent seepage into the cabinet and manual storage compartment. Do not allow "409" or similar cleaners to remain on the finish any longer than necessary.

SECTION 5 - CORRECTIVE MAINTENANCE

Modular Maintenance Method

The back up electronics option allows for user maintenance. The only equipment needed is a screwdriver to fit the cover and clamp screws. The diagnostics outlined in Appendix A should be used to determine the type of fault.

Once the type of fault is isolated the following steps should be taken:

1. If the power supply indicates a power fault which cannot be reset, replace the memory chassis.
2. If the problem seems isolated to only one particular block of memory, use the back-up module select switches to replace that block with the spare module.
3. If the problem is associated with all memory modules, replace the following equipment in the order listed. After each substitution, recheck the error condition.
    1. Memory control board
    2. Receiver-driver box
    3. Memory chassis

Should the procedures outlined above fail to cure the problem, contact CHI Customer Engineering for further assistance.

CAUTION: No attempt should be made to repair a core module core stack. The techniques required are available only at the factory level.

Chassis Board Replacement

CAUTION: Be sure both the CPU and 1106 are off before disconnecting any part of the system.

Access to the chassis boards is obtained by removing the cover to the card rack. It is important that this cover is replaced to ensure adequate cooling.

To remove the control board (uppermost position), the signal cable must be disconnected by pulling the edge connector (J3) off the board. Be sure this connector is squarely seated when the new board is installed.

The bottom position (no receptacle at rear) may be conveniently used for spare board storage.

Receiver-driver Box Replacement

Before proceeding, note the position of the box in relation to the CPU gate hinge so that the new box will be correctly placed. Unscrew the four box cover retaining screws and lift off the cover. The three edge connectors may now be pulled off the circuit board. To remove the box, grasp the metalwork and pull straight out, breaking the grip of the Velcro fasteners.

To install the spare, position the box correctly and press down on the metalwork to engage the Velcro fasteners. When doing this, be careful not to push on the circuit board or its components. Seat the connectors squarely, and attach the cover to retain them.

CAUTION: When closing the 1131 gate, make sure that there is good clearance between 1106 components and CPU components.

Power Supply

The power supply is replaced by exchanging the chassis as follows:

1. Remove card bay covers on both chassis.
2. Remove all boards and install in standby chassis.
3. Transfer signal cable and power cord to standby chassis.
4. Replace covers.

SECTION 6 - THEORY OF OPERATION

Part 1 - System General Description

Figure 7 illustrates the relationship between the CPU and the circuits of the 1106.

Receiver-driver Box (RDB)

The RDB provides interfacing between the processor and the 1106 memory control board in three ways: (1) The signals are amplified and coupled to the 1106 signal cable (hence the name RDB), (2) Read, write and address data are time-multiplexed to 18 cable lines called "The Bus", and (3) CPU control signals are logically combined to form 1106 control signals. In addition, address bits 0, 1 and 2 are generated from CPU signals; these are not always available on some processors with smaller memories.

CPU Interface Cable

The CPU interface cable connects the RDB to the proper CPU circuit points. Jumpers are used in conjunction with the cable whenever a wire does not have at least one end connected to the RDB, e.g. where CPU lamps are connected to CPU signals for customer use.

Memory Control Board (MCB)

The MCB develops the specific control signals needed to

activate the core modules, stores the address data during a read/write cycle, and complements the RDB by multiplexing signals at the 1106 end of the signal cable. The MCB additionally provides an isolated inhibit current source for each core bit.

Core Module(s) (CM)

Figure 8 shows the basic circuits on each CM. Addressing circuits select the storage location by means of current thru two wires on a X-Y grid basis. Inhibit circuits block the magnetic fields of the X-Y lines on whichever of the bit planes a binary zero is to be written. Sense amplifiers are used to detect pulses from cores "containing" zeroes when the X-Y currents are reversed during the read cycle. These pulses are lengthened by buffers for utilization by the MCB.

Control and timing circuits govern the signal sequence to match the magnetic characteristics of the cores.

Power Supply

Three basic supplies operate the 1106, sharing a common power transformer. The filter board reduces ripple to levels acceptable to the regulator board and provides fuse protection.

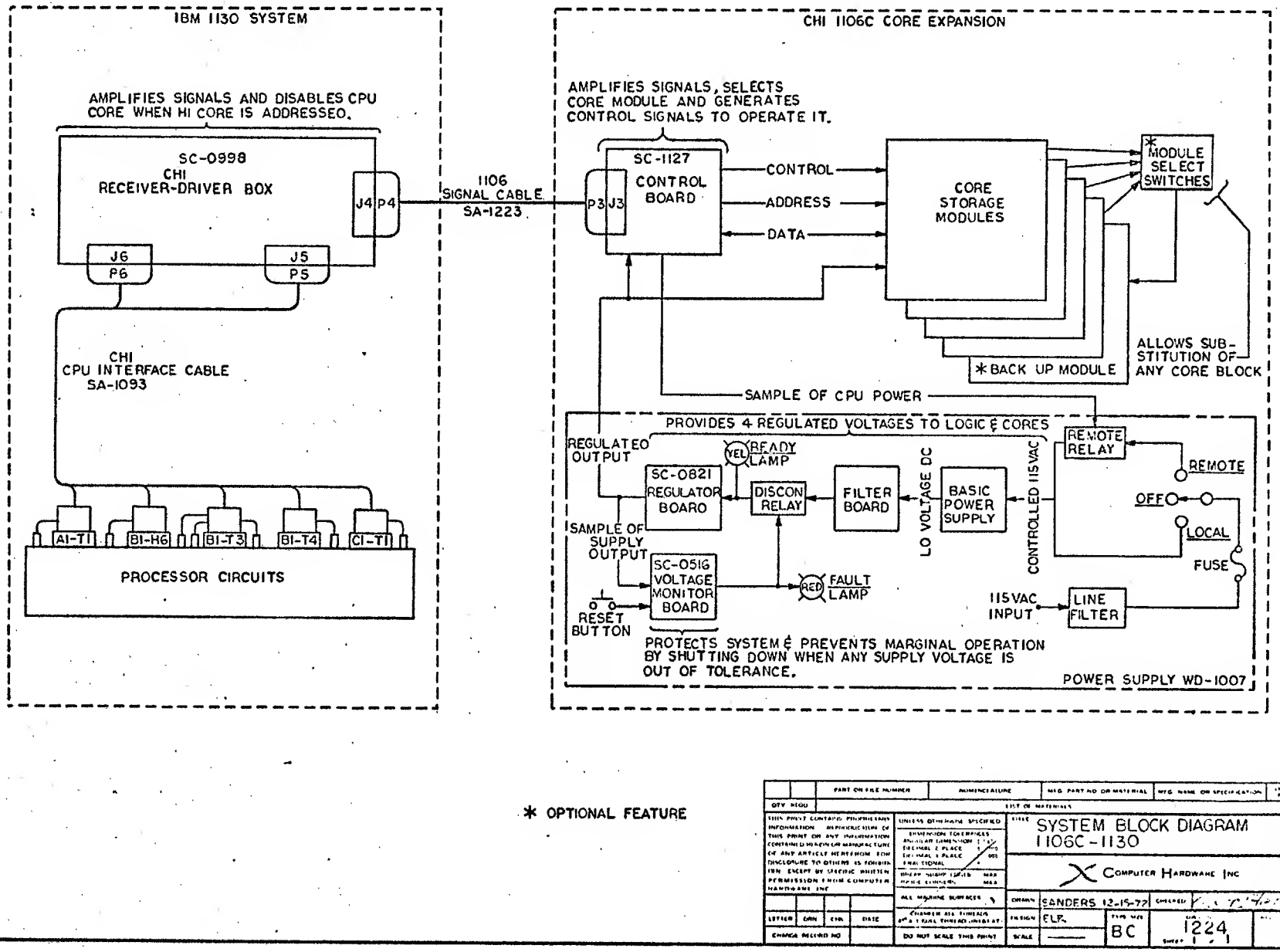
The regulator boards contain components which generate inexact but stable reference voltages. The outputs of the supplies are compared to these references and error signals are developed if they are not exactly equal. Adjustable proportioning circuits are set at the factory so that the magnitude of the error signal

will produce an exact and stable final output. In addition,the circuitry limits the current drawn to preset maximums in the event of a fault.

A heat sink assembly contains the power transistors which are the actual means of controlling the supply outputs. It is considered part of the regulator board in Figure 7.

A voltage monitor board controls a disconnecting relay on the filter board. Should voltages deviate beyond set limits, the relay will lock in to shut down the supply.

In the remote mode, the AC is controlled by a relay. This is in turn operated by a sub-miniature relay on the MCB which is slaved to the CPU power system.



* OPTIONAL FEATURE

	PART OR FILE NUMBER	NOMENCLATURE	MFG PART NO OR MATERIAL	MFG NAME OR SPECIFICATION	ITEM NO
QTY REQD	LIST OF MATERIALS				

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DECIMAL 4 PLACE
FRACTIONAL
BREAK SHARP EDGES MAX
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ALL MACHINE SURFACES
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DESIGN: ELP
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TYPE NO: BC
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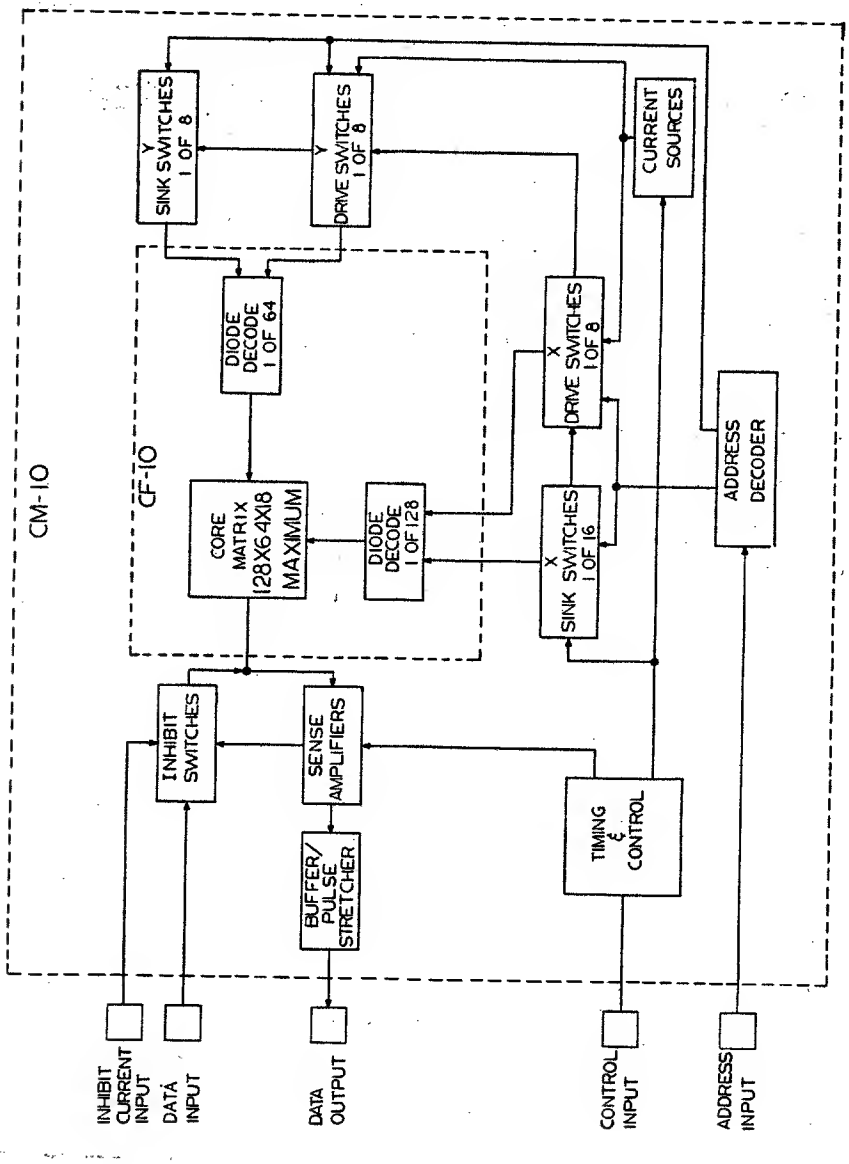
SHEET 1 OF 1

BC 1224

FIGURE 7



CORE MODULE BLOCK DIAGRAM

FIGURE 8

Part 2 - Interface Logic

Preface

1. Because the technician will be viewing the operation of the 1106 as a sequence of signals, this description is presented in that manner. Therefore, a signal may appear more than once if both transitions are significant.
2. The titles "Receiver-Driver Box", "Memory Control Board", and "Core Module" have been abbreviated to "RDB", "MCB", and "CM", respectively.
3. Clock times are not referenced unless a definite relationship, such as that obtained by gating, exists.
4. Unless otherwise noted, timing circuits may vary up to +- 100% and still operate. Their main value is to provide a wide safety margin to allow for circuit and environmental variables.
5. The number preceeding each signal description refers to the similarly numbered points on the timing diagram (Figure 7). Signals occuring together, or within 40ns, share the same number.
6. Signal names not preceeded by "CPU" indicate signals generated by 1106 circuitry.

Signal Sequence (refer to Figure 9, Timing Diagram)

1. CPU ADDRESS BITS 0-17 are presented to the MCB between

memory cycles; this is the "resting" condition of the bus. During this time, any change in the CPU storage address register will be propagated to the MCB addressing circuitry. The address, however, is not relevent until the beginning of a memory cycle.

2. CPU STORAGE READ GATE (RDB, IC 6-2) signals the beginning of a CPU memory cycle at TØ. However, because of the inherent speed of the 1106 CM(s), READ CYCLE cannot be used to begin an 1106 cycle directly. It is used to trigger the read delay O.S., which will later start the 1106 read/write cycle in synchronism with the CPU.

3. MEMORY CYCLE (RDB, IC 13-5; MCB, IC 23-5) marks the expiration of the read delay (RDB, IC 7-12) after 100ns, 400ns or 600ns for 2.0-, 2.25- or 4.0- usec 1801/1802's, respectively. Because RDB and MCB circuits must operate together, no use will be made of this signal at the RDB until it has traversed the signal cable some 35ns later.

3. READ STROBE (MCB, IC 21-6) is a pulse generated by MEMORY CYCLE triggering the read strobe O.S. It commands a CM to begin a readout cycle. The 220ns strobe length as well as the time to actual data output is dictated by the requirements of the CM circuitry and must be within 10%.

3. ENABLE ADDRESS LATCH (MCB, IC 25-11) locks in the address data at the start of the read cycle. The output of the latches is used to select the CM and specific core location.

4. ENABLE SENSE (RDB, IC 8-4) is a pulse generated by the enable sense O.S. to form a 300ns-wide window at the RDB end of the

bus. C19 delays the window by 30ns to allow the bus to settle after the address data is removed.

5. MEMORY DATA BITS 1-18 (CM & MCB) output from the CM and pass into the bus 200ns after the sense window opens.

5. SENSE AMP BITS 0-17 (RDB), delayed by the cable, appear at the 1131/1106 interface about 235ns after the sense window opens. Although MEMORY DATA BITS 1-18 continue well into the write cycle (over 1 usec), the expiration of the enable sense O.S. closes the sense window after only 150ns. The result is a sense pulse that resembles that of the CPU in timing (T2) and duration (100ns).

It should be apparent that because (1) the leading edge of READ STROBE determines when the CM will output memory data, and (2) the trailing edge of ENABLE SENSE determines the end of the sense window, the sense pulse can be tightly controlled if necessary. The read strobe and sense enable O.S.'s set the leading and trailing edges, respectively, so that it is possible to exactly align the 1106 output with that of 1131 by slightly altering the O.S. capacitors. This procedure is rarely required.

Observation of the congruity of CPU and 1106 sense pulses may be made at SENSE BITS 0-17 with the 1131 in the storage load mode. This mode repeatedly excercises the two core systems as the addressing increments through low and high core.

6. CPU STORAGE WRITE CYCLE (RDB, IC 4-12) signals the beginning of a CPU write cycle at T4. However, because the 1106 write

cycle must be terminated early to allow for the addressing "cycle", it is not used directly. Instead it triggers the write cycle O.S.

6. WRITE CYCLE (RDB, IC 12-15) is a shortened version (750 vs 1100-1800ns) of CPU STORAGE WRITE CYCLE. It begins an 1106 write cycle in synchronism with the CPU at T4.

6. ENABLE CONTROL DATA (RDB, IC 8-12) connects B BITS 0-17 (write data) to the RDB end of the bus at T3. No action is required at the MCB end, because the CM performs its own gating.

6. RESET MEMORY DATA (MCB, IC 25-8) is restored 40ns later when WRITE CYCLE reaches the MCB. The memory data latches are thereby removed from the bus for the remainder of the CPU memory cycle.

7. WRITE STROBE (MCB, IC 21-8) is a pulse generated by the expiration of the write delay O.S. triggering the write strobe O.S. It commands a CM to begin its write cycle. The 220ns delay allows the bus to settle before the write data is used. The 300ns strobe length must be within 10%.

8. WRITE CYCLE (RDB, IC 12-15) goes inactive at the expiration of the write cycle O.S. signifying the end of the 1106 write cycle.

8. ENABLE CONTROL DATA (RDB, IC 8-12) removes the write data from the RDB end of the bus.

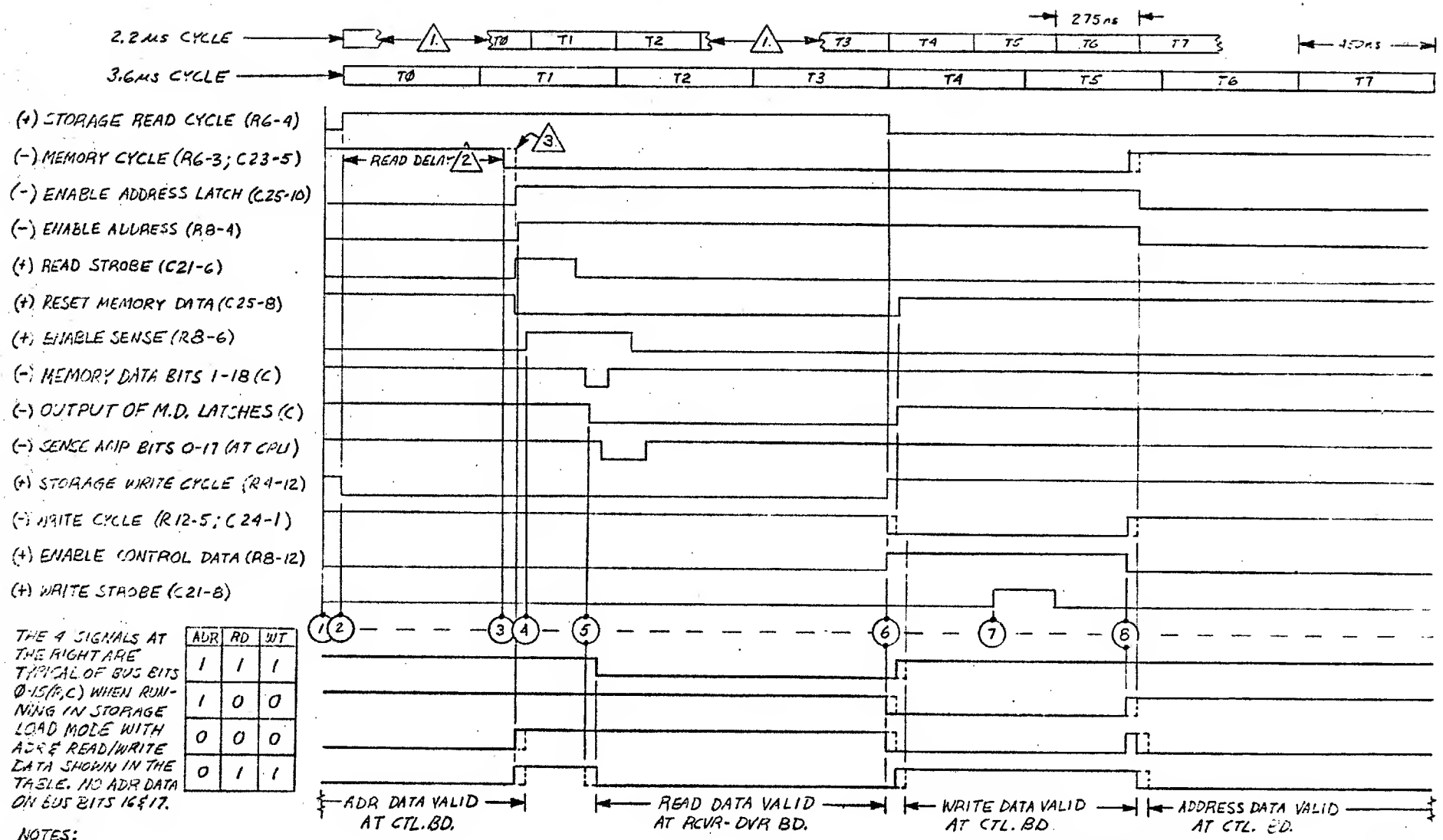
8. MEMORY CYCLE (MCB, IC 23-5) is terminated by WRITE CYCLE.

8. ENABLE ADDRESS (RDB, IC 8-4) connects CPU ADDRESS BITS 0-15 to the bus.

8. ENABLE ADDRESS LATCH (MCB, IC 25-11) reopens the address latches to the bus. The time until the next read cycle (140 or 540ns minimum) allows the address data on the bus to settle.

Data Save

When the CPU is powering down, signals to the 1106 become unstable long before the 1106 power supply relays can shut down the unit. During this time parity-incorrect Write Cycles or Read cycles without the corresponding restoring Write Cycles could occur. To prevent this, a comparator is used to generate DATA SAVE (MCB, IC 29-7) when the +6V SENSE Signal drops below +5VDC. DATA SAVE is applied to all core modules and prevents any further Read/Write Cycles.



THE 4 SIGNALS AT THE RIGHT ARE TYPICAL OF BUS BITS Ø-15(P,C) WHEN RUNNING IN STORAGE LOAD MODE WITH ADR & READ/WRITE DATA SHOWN IN THE TABLE. NO ADR DATA ON BUS BITS 16&17.

ADR	RD	WT
1	1	1
1	0	0
0	0	0
0	1	1

NOTES:

1. FOR A 2.2μs CYCLE, THESE PORTIONS OF THE DIAGRAM SHOULD BE COMPRESSED.
2. ≈150ns FOR 2.2μs 1131; ≈500ns FOR 3.6μs 1131.
3. WHERE SIGNALS ARE COMMON TO RCVR-DVR. BD. & MEM. CTL. BD., THE SIGNAL AT THE LATTER IS SHOWN DASHED.

SIGNAL LOCATION LEGEND

R= RCVR-DVR BD.
C= MEM. CTL. BD
IC NUMBER (X 24-3) PIN NO.

CMI
19 JAN 73 LGW

1106C INTERFACE TIMING DIAGRAM

FIGURE 9

Part 3 - Core Module Magnetics

The core stack assembly, mounted centrally on the CM contains the lithium-nickel ferrite core arrays positioned between two hinged P.C. boards. The core arrays are affixed to ground planes between the two boards to minimize thermal gradients in the core area. Diode decode matrices for the X and Y axes are located at the core stack periphery.

A thermistor is provided to sense core temperatures. The thermistor becomes a part of a servo loop in the stack drive electronics to compensate for variations in core characteristics with temperature changes.

The core stack is electrically organized as a 3D, 3 wire coincident-current core stack. A memory data word is addressed for read or write by applying one half of the required core switching current on one selected X line and one half on one selected Y line. There are 128 X axis and 64 Y axis drive lines for a total of 8192 word intersections. The core performs the AND logic function in the address selection process, because only when X and Y currents are present in the core aperture will the core be selected.

One of 64 drive lines on each axis is selected via an 8 X 8, two-diode-per-line selection matrix. The third line through the memory cores is used as the common sense-inhibit line for the During read time the sense-inhibit line is used to sense the flux reversal in the core. During write time the sense-inhibit line

is used to inhibit the X and Y currents from setting a core to the "1" state, if "0" is to be written. The magnitude and direction of the inhibit current is such that the net magnetic field is not sufficient to flip the core. In effect the "AND gate" (core) is blocked. Conversely, when "1" is to be written, the inhibit line is not energized. Eighteen sense/inhibit lines are used to read and write the data pattern at the location selected by the coincidence of X and Y currents.

Part 4 - Core Module Electronics

The CM contains the circuitry required to drive and sense the core stack. To function, it requires READ and WRITE pulse inputs to generate read and write memory half cycles, respectively. Timing signals generated within the CM are factory set and should not require readjustment for the life of the equipment.

Timing and Control Signals

1. RTD and RTS are current pulses of durations approximately equal to that of the READ timing pulse input and are used to close selected drive and sink switches in the X and Y stack drive circuits. For example, RTDX closes 1 of 8 read-drive floating switches composed of CR17, T17 and Q26. Address decoder IC13 performs the 1 of 8 switch selection. RTSX, RTDY and RTSY perform in a similar manner.
2. WTD and WTS perform the same function as RTD and RTS, but occur during a write half cycle.
3. Strobe is a short positive pulse to the sense amplifiers which occurs approximately at core peaking time during a read half cycle. Strobe is generated by the timing circuits associated with Q21, Q22 and Q23.
4. TZ is a timing pulse enabling input data to control the inhibit current switches. The duration of TZ is approximately equal to that of the WRITE pulse input plus 70ns, the delay time of DL2.

X and Y Drive Circuits

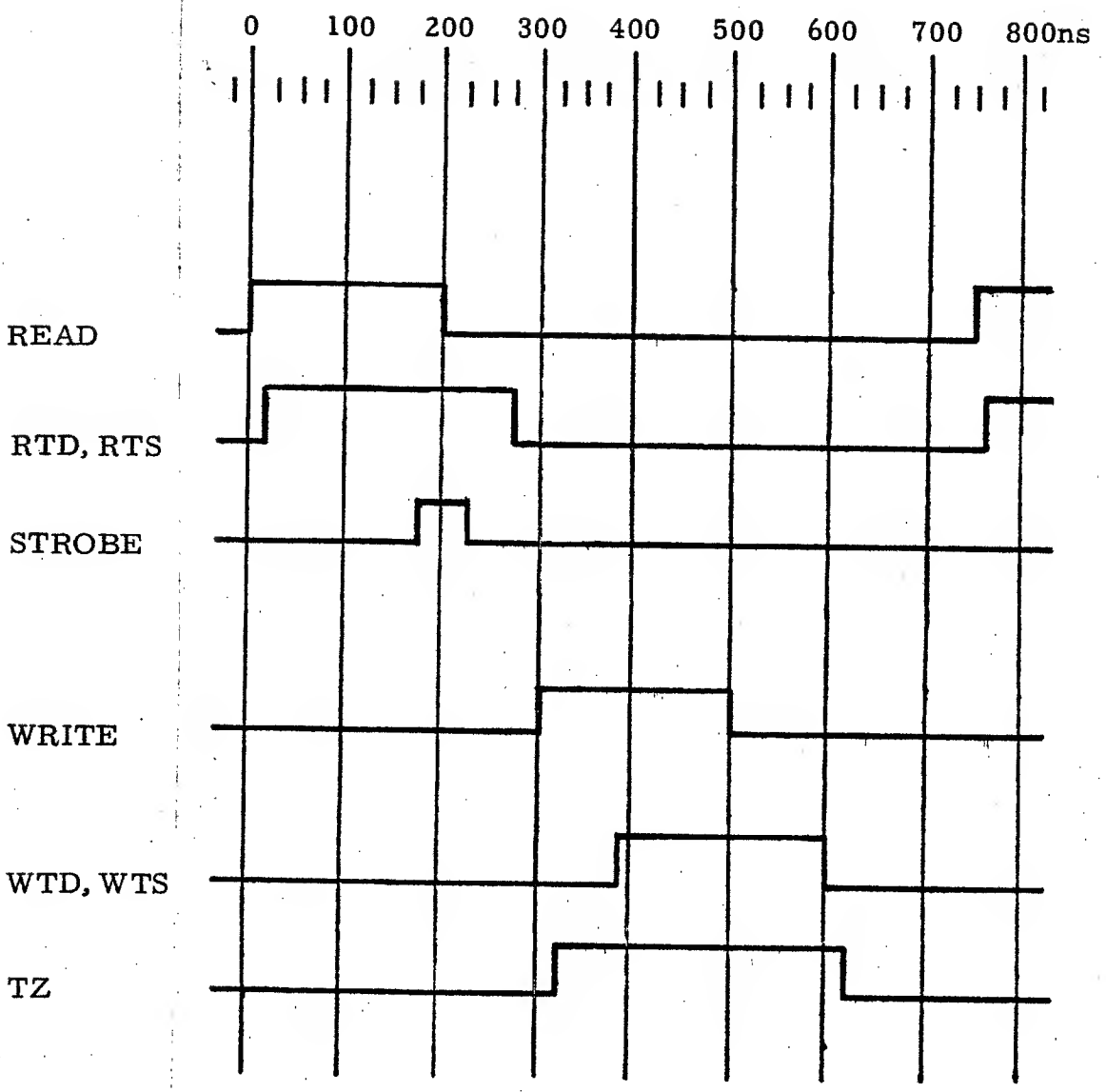
X and Y drive currents to the core stack are controlled in magnitude and rise time by two linear, active current sources composed of Q14, Q16 and Q19 and associated components. R50 and C19 form an R-C integrator to control current rise times. Q12 clamps the current magnitudes to a value established by the core stack thermistor to provide current-versus-temperature compensation. Current source outputs are routed to stack drive and sink switch transistors at the core stack periphery by an eight-transformer distribution matrix.

Data Circuits

Core stack signal sensing is performed by a dual-channel integrated circuit sense amplifier (IC6). The sense lines are terminated by R21. Pins 4 and 5 of IC6 are inputs to a reference amplifier which sets the threshold for identical amplifiers at pins 2-3 and 6-7 of the same IC. Signal threshold is developed across R15 by a precision voltage divider network.

The strobe pulse to the sense amplifier gates the sense amplifier at read time and enables data read-out of the core stack to be transferred to the data output buffers, Q5 and Q6. Q5 and Q6 are fast-on, slow-off devices to effectively stretch the $\overline{\text{Memory Data}}$ ($\overline{\text{MD}}$) output pulse width.

Inhibit switches (Darlington pairs Q_1 - Q_3 and Q_2 - Q_4 supply inhibit currents from remote inhibit resistors to the center-tapped sense/inhibit lines. The inhibit switches are controlled by input data, Control Data ($\overline{\text{CD}}$), as timed by TZ during a write cycle.



CORE MODULE TIMING DIAGRAM

FIGURE 10

Part 5 - Power Supply

Basic Supplies (Wiring Diagram WC-1007, Figure 14)

T1, D1-D3 and C1-C3 provide unregulated -20, +20 and +8V for the -15, +15 and +5V supplies, respectively. R1-R3 limit rectifier currents when power is applied. R4-R6 act to discharge the filters when power is removed.

-15 Regulator (Schematic Diagram SC-0821)

The -15V output is sampled by the voltage divider R38-40. Differential pair Q11-Q12 compare the sample to the 7.5V reference zener D4. If an increase occurs in the output, Q11 will conduct more heavily, causing the emitter of Q12 to become more negative. With the base of Q12 held at +7.5V, the bias will result in heavier conduction through Q12, R35 and R36. As the R35-R36 junction becomes less negative, Q14 conducts more heavily.

Q14's rising output is applied to the base of Q3, the pass transistor, which conducts less and lowers the output voltage to the nominal value. A drop in output voltage results in similar but opposite circuit action. R39 is adjusted for an output of exactly -15V.

Should an excessive current be drawn, the voltage drop across R46 biases Q15 into conduction through base-current-limit resistor R44. Q15's output is applied to Q14 to reduce the

output voltage available from the supply. Thus a maximum fault current of 3 amps (current limit point) can be drawn from the supply without causing a considerable drop in the voltage. The supply must support such an overload only until F1 blows or the voltage monitor reacts to the drop in output.

When power is first applied, Q14 does not have sufficient base current to turn on the pass transistor. To "start up" the circuit, the now low output voltage is applied to the emitter of Q13, whose base is fixed at -20V. This bias causes Q13 to conduct and supply the needed current to Q14. When the output line rises to -15, D5 turns off Q13.

+15 Regulator

The +15 regulator performs in a like manner with the exception that the reference source of IC1 (VREF) is used instead of a zener.

+5 Regulator

IC1 performs the comparisons of Q11-Q12 and the current limiting action of Q15 in the -15V supply. VREF, typically 7.15 volts, is divided down to 5 volts and is compared to a full voltage sample of the +5 output. A separate +5 SENSE line runs to the motherboard to insure that the output is accurate at the load. R4-C1 prevent damage to the supply should the sense line open.

The frequency compensation port of IC1 is additionally used to protect the IC. D6-D7-D1 and D2 monitor the +8V UNREG and +15V, respectively, and shut IC1 down should either voltage fail. Without this feature, IC1 would interpret the supply loss as an error in supply output and try to compensate by increasing its output current beyond its maximum rating.

+3 Regulator

The +3 regulator obtains its reference from the +5 SENSE line. The output is fixed by the 3-to-5 division ratio of R13-R16. The current thru R18 from the +15 supply is sufficient to start up the circuit without the aid of a start up transistor.

Ratings

Output Voltage	Regulation	Maximum Operating Current	Current Limit
+15	1%	7.5A.	9A.
-15	1%	2A.	3A.
+ 5	1%	6A.	9A.
+ 3	10%	1A.	None

Voltage Monitor (Figures 16, 17)

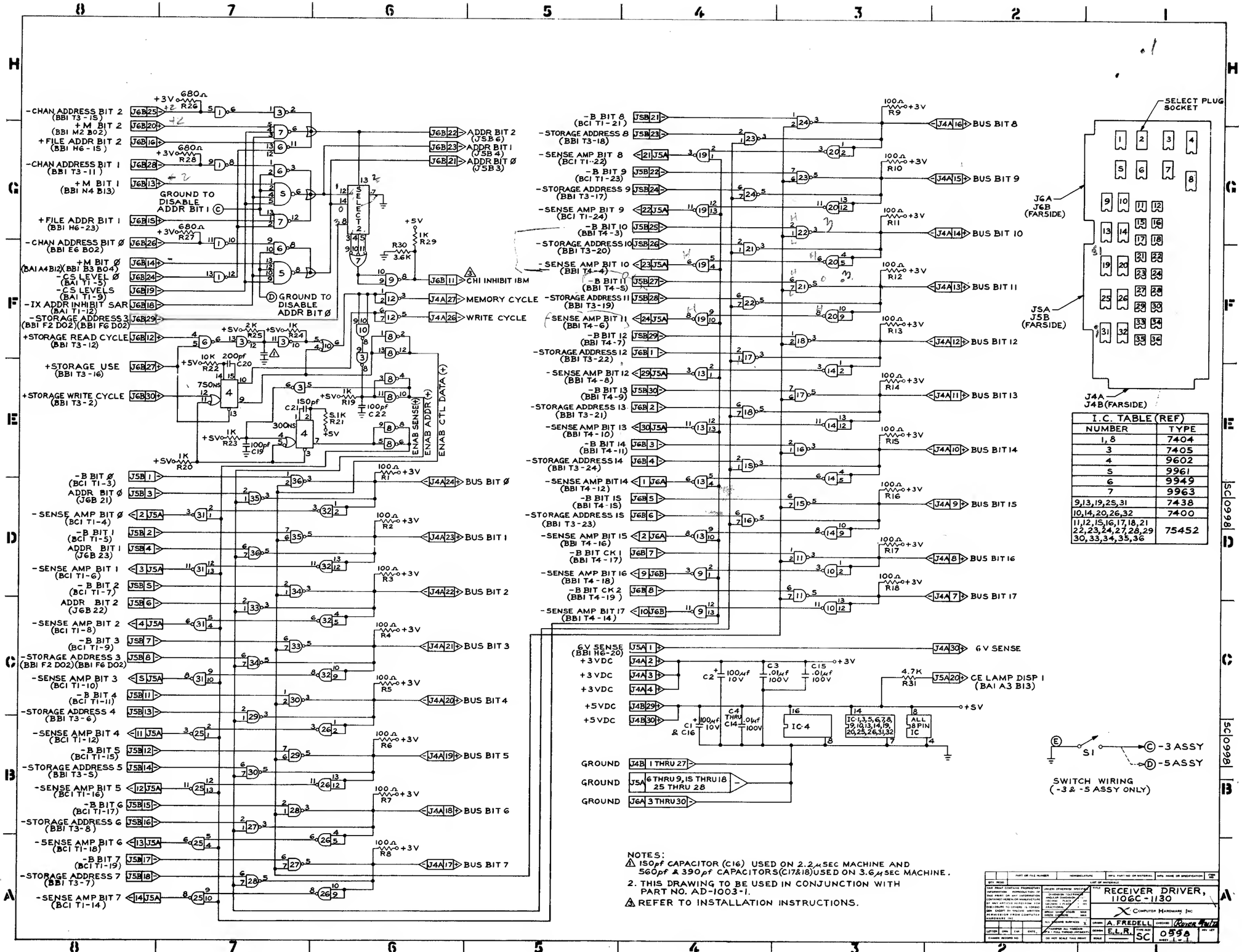
Q10, Q9, Q8, Q14 and Q7-13 compare the monitored voltages (or samples thereof) to reference voltages for deviations in one direction. The voltage limits are set by fixed circuit values except that R30 sets the limits in the +5 undervoltage circuit. When a limit is exceeded, the error signal rises

above one volt, passes through Q11 and triggers Q6. Q6 energizes the disconnect relay on the filter board to turn off all supplies.

Q6 is reset by Q16 shorting it out. R32-C5 suppress a voltage spike that would retrigger Q6 at the end of reset. D9 shunts the excess reverse bias on Q16 when Q6 fires; without D9, C5, charged to the relay supply, would discharge (reverse current) through Q16, R32 and Q6. D10 and D8 create a voltage drop sufficient to supply the fault reset pushbutton while Q6 is fired.

The feedback from Q5 to the +5 voltage divider biases the divider to hold the circuit in the error condition. If R30 is properly adjusted, Q6 fires when the +5 drops to 4.75V, but the error signal will not turn off until the +5 rises to 4.82V. This hysteresis prevents oscillation if the +5 remains at the trip voltage for any length of time.

During start-up Q11 blocks the error signal from reaching Q6 for about five seconds. The delay is caused by C7 shutting off Q12 until it is charged. D6 sets Q12's current by preventing C7's charge from rising to more than 5.1V. After the delay, Q12's current is sufficient to saturate Q11 and allow error signals to pass.



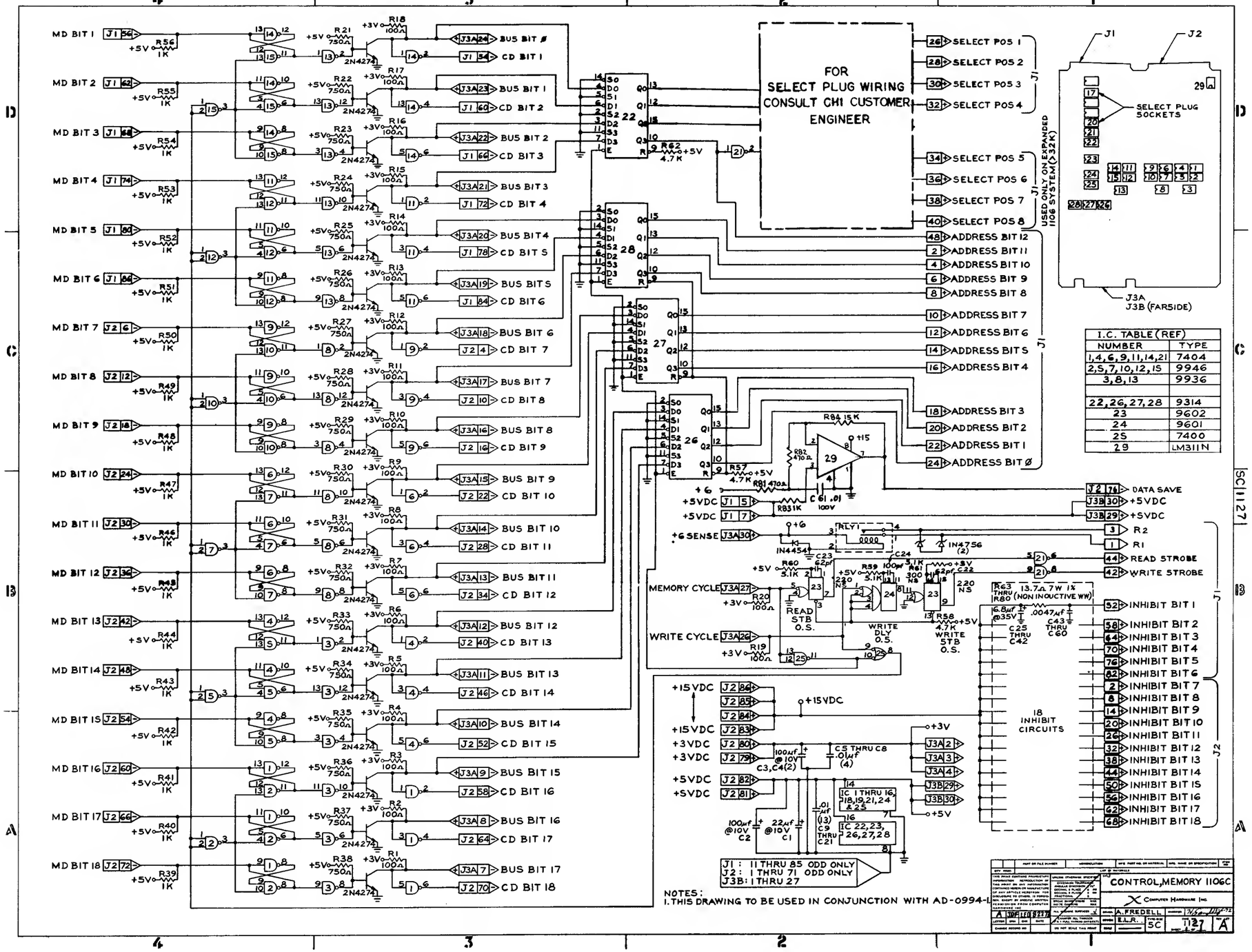
I.C. TABLE (REF)	
NUMBER	TYPE
1, 8	7404
3	7405
4	9602
5	9961
6	9949
7	9963
9,13,19,25,31	7438
10,14,20,26,32	7400
11,12,15,16,17,18,21 22,23,24,27,28,29 30,33,34,35,36	75452

NOTES:
1. ⚠ 150pf CAPACITOR (C16) USED ON 2.2μSEC MACHINE AND 560pf & 390pf CAPACITORS (C17&18) USED ON 3.6μSEC MACHINE.
2. THIS DRAWING TO BE USED IN CONJUNCTION WITH PART NO. AD-1003-1.
3. ⚠ REFER TO INSTALLATION INSTRUCTIONS.

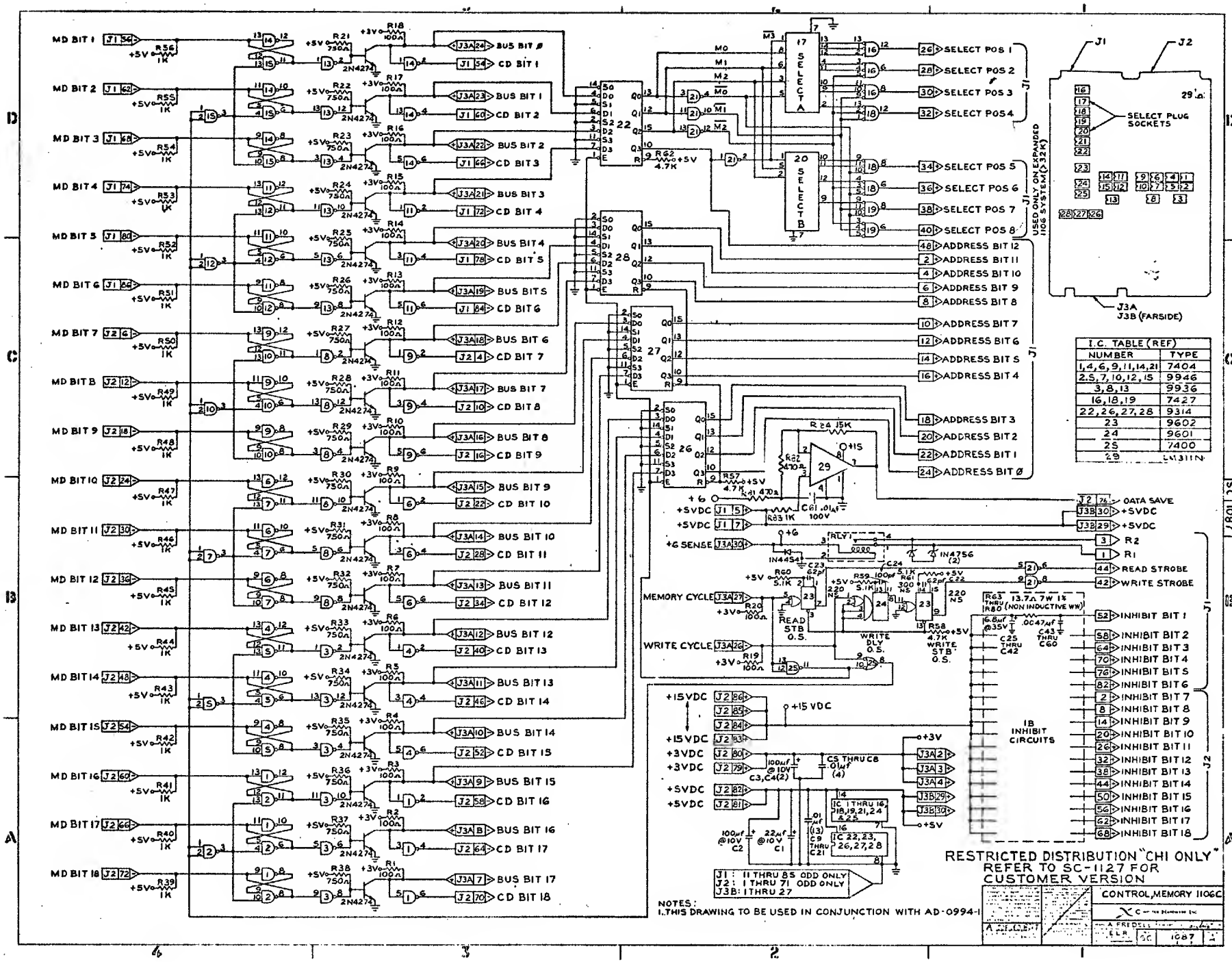
TITLE	RECEIVER DRIVER, 1106C-1130		
	COMPUTER HARDWARE INC		
DRAWN	A. FREDELL	CHECKED	Roger Smith
DESIGN	E.L.R.	TYPE-SIZE	SC
SCALE		SHEET	0998 1 of 1

SC0998 D SC0998 C SC0998 B

FIGURE 11


MD BIT 1 J1 54
MD BIT 2 J1 62
MD BIT 3 J1 68
MD BIT 4 J1 74
MD BIT 5 J1 80
MD BIT 6 J1 84
MD BIT 7 J2 6
MD BIT 8 J2 12
MD BIT 9 J2 18
MD BIT 10 J2 24
MD BIT 11 J2 30
MD BIT 12 J2 36
MD BIT 13 J2 42
MD BIT 14 J2 48
MD BIT 15 J2 54
MD BIT 16 J2 60
MD BIT 17 J2 66
MD BIT 18 J2 72
BUS BIT 1
CD BIT 1
BUS BIT 2
CD BIT 2
BUS BIT 3
CD BIT 3
BUS BIT 4
CD BIT 4
BUS BIT 5
CD BIT 5
BUS BIT 6
CD BIT 6
BUS BIT 7
CD BIT 7
BUS BIT 8
CD BIT 8
BUS BIT 9
CD BIT 9
BUS BIT 10
CD BIT 10
BUS BIT 11
CD BIT 11
BUS BIT 12
CD BIT 12
BUS BIT 13
CD BIT 13
BUS BIT 14
CD BIT 14
BUS BIT 15
CD BIT 15
BUS BIT 16
CD BIT 16
BUS BIT 17
CD BIT 17
BUS BIT 18
CD BIT 18
FOR SELECT PLUG WIRING CONSULT CHI CUSTOMER ENGINEER
SELECT POS 1
SELECT POS 2
SELECT POS 3
SELECT POS 4
SELECT POS 5
SELECT POS 6
SELECT POS 7
SELECT POS 8
USED ONLY ON EXPANDED 1106 SYSTEM (>32K)
ADDRESS BIT 12
ADDRESS BIT 11
ADDRESS BIT 10
ADDRESS BIT 9
ADDRESS BIT 8
ADDRESS BIT 7
ADDRESS BIT 6
ADDRESS BIT 5
ADDRESS BIT 4
ADDRESS BIT 3
ADDRESS BIT 2
ADDRESS BIT 1
ADDRESS BIT Ø
J1
J2
SELECT PLUG SOCKETS
J3A
J3B (FARSIDE)
I.C. TABLE (REF)
NUMBER TYPE
1,4,6,9,11,14,21 7404
2,5,7,10,12,15 9946
3,8,13 9936
22,26,27,28 9314
23 9602
24 9601
25 7400
29 LM311N
DATA SAVE
+5VDC
+5VDC
R2
R1
READ STROBE
WRITE STROBE
MEMORY CYCLE
WRITE CYCLE
READ STB O.S.
WRITE DLY O.S.
WRITE STB O.S.
INHIBIT BIT 1
INHIBIT BIT 2
INHIBIT BIT 3
INHIBIT BIT 4
INHIBIT BIT 5
INHIBIT BIT 6
INHIBIT BIT 7
INHIBIT BIT 8
INHIBIT BIT 9
INHIBIT BIT 10
INHIBIT BIT 11
INHIBIT BIT 12
INHIBIT BIT 13
INHIBIT BIT 14
INHIBIT BIT 15
INHIBIT BIT 16
INHIBIT BIT 17
INHIBIT BIT 18
18 INHIBIT CIRCUITS
+15VDC
+3VDC
+5VDC
J1 : 11 THRU 85 ODD ONLY
J2 : 1 THRU 71 ODD ONLY
J3B: 1 THRU 27
NOTES:
1. THIS DRAWING TO BE USED IN CONJUNCTION WITH AD-0994-I
CONTROL, MEMORY 1106C
COMPUTER HARDWARE INC.
A. FREDELL
E.L.R.
SC 1127 A
SC11127

7-2 FIGURE 12


MD BIT 1
MD BIT 2
MD BIT 3
MD BIT 4
MD BIT 5
MD BIT 6
MD BIT 7
MD BIT 8
MD BIT 9
MD BIT 10
MD BIT 11
MD BIT 12
MD BIT 13
MD BIT 14
MD BIT 15
MD BIT 16
MD BIT 17
MD BIT 18
BUS BIT Ø
CD BIT 1
BUS BIT 1
CD BIT 2
BUS BIT 2
CD BIT 3
BUS BIT 3
CD BIT 4
BUS BIT 4
CD BIT 5
BUS BIT 5
CD BIT 6
BUS BIT 6
CD BIT 7
BUS BIT 7
CD BIT 8
BUS BIT 8
CD BIT 9
BUS BIT 9
CD BIT 10
BUS BIT 10
CD BIT 11
BUS BIT 11
CD BIT 12
BUS BIT 12
CD BIT 13
BUS BIT 13
CD BIT 14
BUS BIT 14
CD BIT 15
BUS BIT 15
CD BIT 16
BUS BIT 16
CD BIT 17
BUS BIT 17
CD BIT 18
SELECT POS 1
SELECT POS 2
SELECT POS 3
SELECT POS 4
SELECT POS 5
SELECT POS 6
SELECT POS 7
SELECT POS 8
ADDRESS BIT 12
ADDRESS BIT 11
ADDRESS BIT 10
ADDRESS BIT 9
ADDRESS BIT 8
ADDRESS BIT 7
ADDRESS BIT 6
ADDRESS BIT 5
ADDRESS BIT 4
ADDRESS BIT 3
ADDRESS BIT 2
ADDRESS BIT 1
ADDRESS BIT Ø
USED ONLY ON EXPANDED I/OS SYSTEM (>32K)
SELECT PLUG SOCKETS
J3A
J3B (FARSIDE)
I.C. TABLE (REF)
NUMBER | TYPE
1,4,6,9,11,14,21 | 7404
2,5,7,10,12,15 | 9946
3,8,13 | 9936
16,18,19 | 7427
22,26,27,28 | 9314
23 | 9602
24 | 9601
25 | 7400
29 | LM311N
DATA SAVE
+5VDC
+5VDC
+G SENSE
R2
R1
READ STROBE
WRITE STROBE
MEMORY CYCLE
WRITE CYCLE
READ STB 0.5.
WRITE DLY 0.5.
WRITE STB 0.5.
INHIBIT BIT 1
INHIBIT BIT 2
INHIBIT BIT 3
INHIBIT BIT 4
INHIBIT BIT 5
INHIBIT BIT 6
INHIBIT BIT 7
INHIBIT BIT 8
INHIBIT BIT 9
INHIBIT BIT 10
INHIBIT BIT 11
INHIBIT BIT 12
INHIBIT BIT 13
INHIBIT BIT 14
INHIBIT BIT 15
INHIBIT BIT 16
INHIBIT BIT 17
INHIBIT BIT 18
18 INHIBIT CIRCUITS
+15VDC
+3VDC
+5VDC
J1 : 11 THRU 85 ODD ONLY
J2 : 1 THRU 71 ODD ONLY
J3B: 1THRU 27
NOTES:
1.THIS DRAWING TO BE USED IN CONJUNCTION WITH AD-0994-I
RESTRICTED DISTRIBUTION "CHI ONLY"
REFER TO SC-1127 FOR CUSTOMER VERSION
CONTROL,MEMORY 1106C
SC 1087

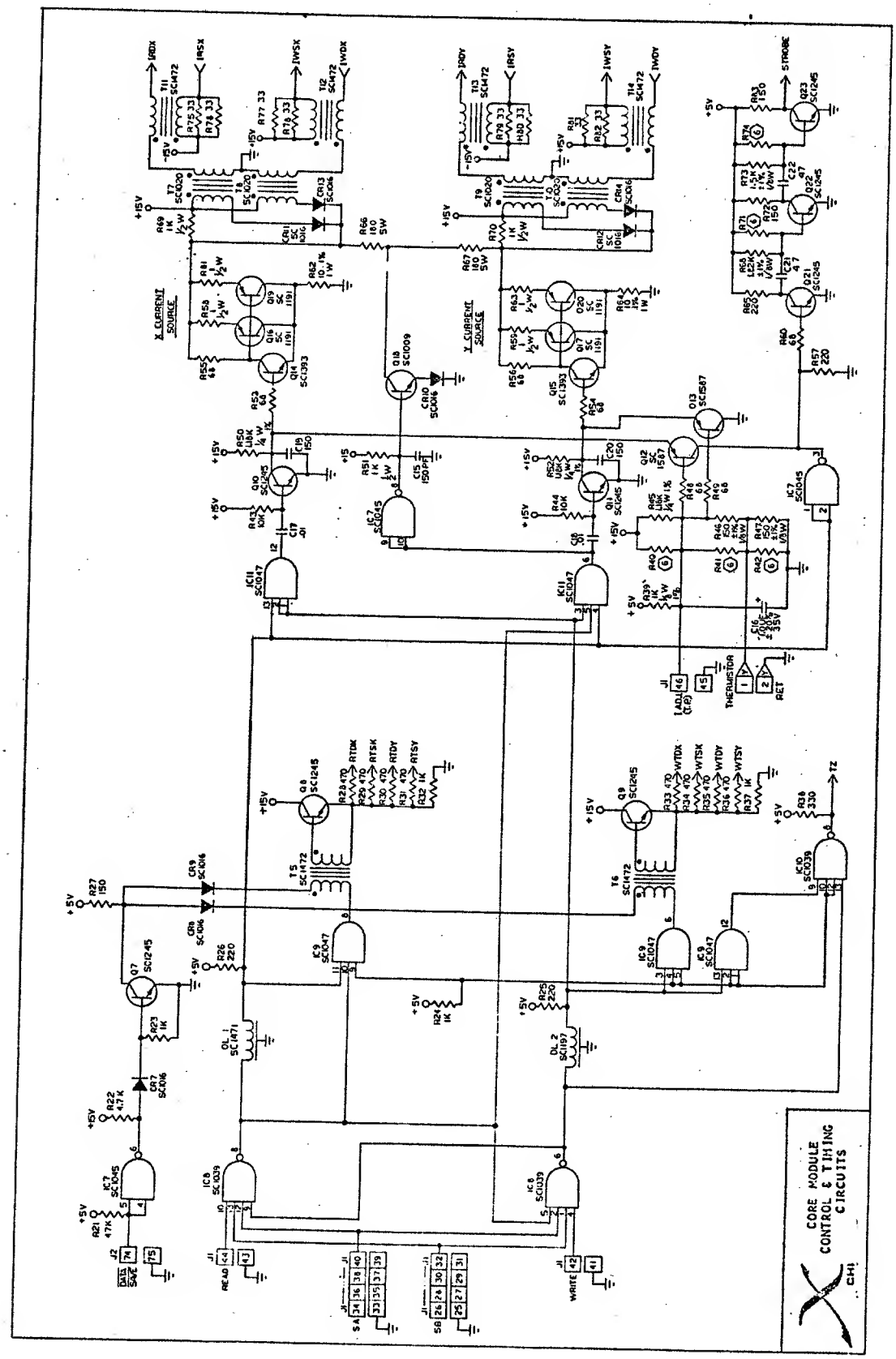

CORE MODULE
CONTROL & TIMING
CIRCUITS
CH1
X CURRENT SOURCE
Y CURRENT SOURCE
THERMISTOR
RET
READ
WRITE
STROBE

FIGURE 13A

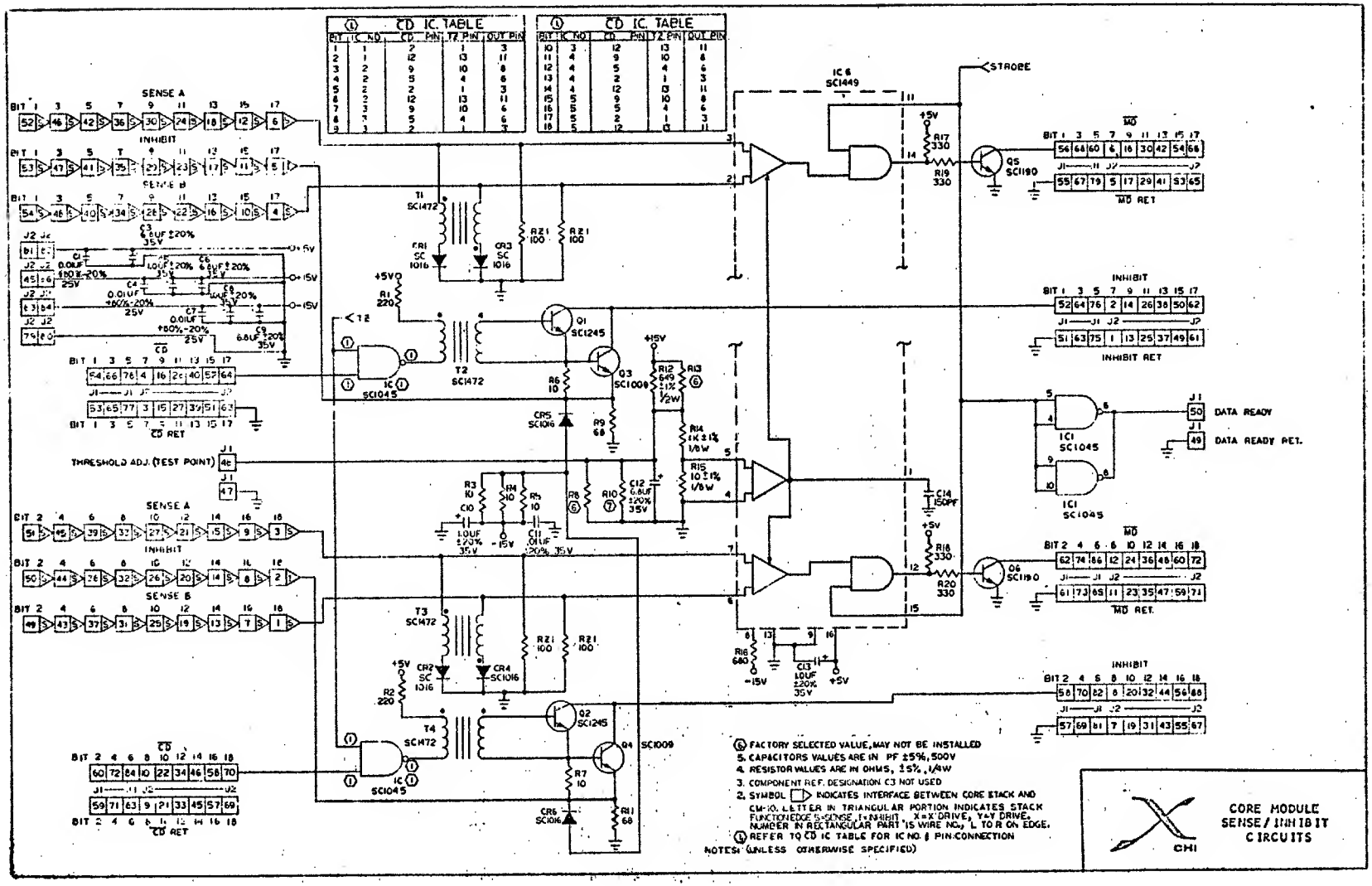

CD IC TABLE
CD IC TABLE
SENSE A
INHIBIT
SENSE B
CD
CD RET
THRESHOLD ADJ. (TEST POINT)
STROBE
IC 6 SC1449
MD
MD RET
INHIBIT RET
DATA READY
DATA READY RET.
T1 SC1472
T2 SC1472
T3 SC1472
T4 SC1472
Q1 SC1245
Q2 SC1245
Q3 SC1009
Q4 SC1009
Q5 SC1190
Q6 SC1190
IC1 SC1045
CR1 SC 1016
CR2 SC 1016
CR3 SC 1016
CR4 SC1016
CR5 SC1016
CR6 SC1016
+5V
+15V
-15V
FACTORY SELECTED VALUE, MAY NOT BE INSTALLED
CAPACITORS VALUES ARE IN PF ±5%, 500V
RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
COMPONENT REF. DESIGNATION C3 NOT USED
SYMBOL INDICATES INTERFACE BETWEEN CORE STACK AND CM-10. LETTER IN TRIANGULAR PORTION INDICATES STACK FUNCTION EDGE S=SENSE, I=INHIBIT X=X DRIVE, Y=Y DRIVE. NUMBER IN RECTANGULAR PART IS WIRE NO., L TO R ON EDGE.
REFER TO CD IC TABLE FOR IC NO. & PIN CONNECTION
NOTES: UNLESS OTHERWISE SPECIFIED)
CHI
CORE MODULE SENSE/INHIBIT CIRCUITS

FIGURE 13B

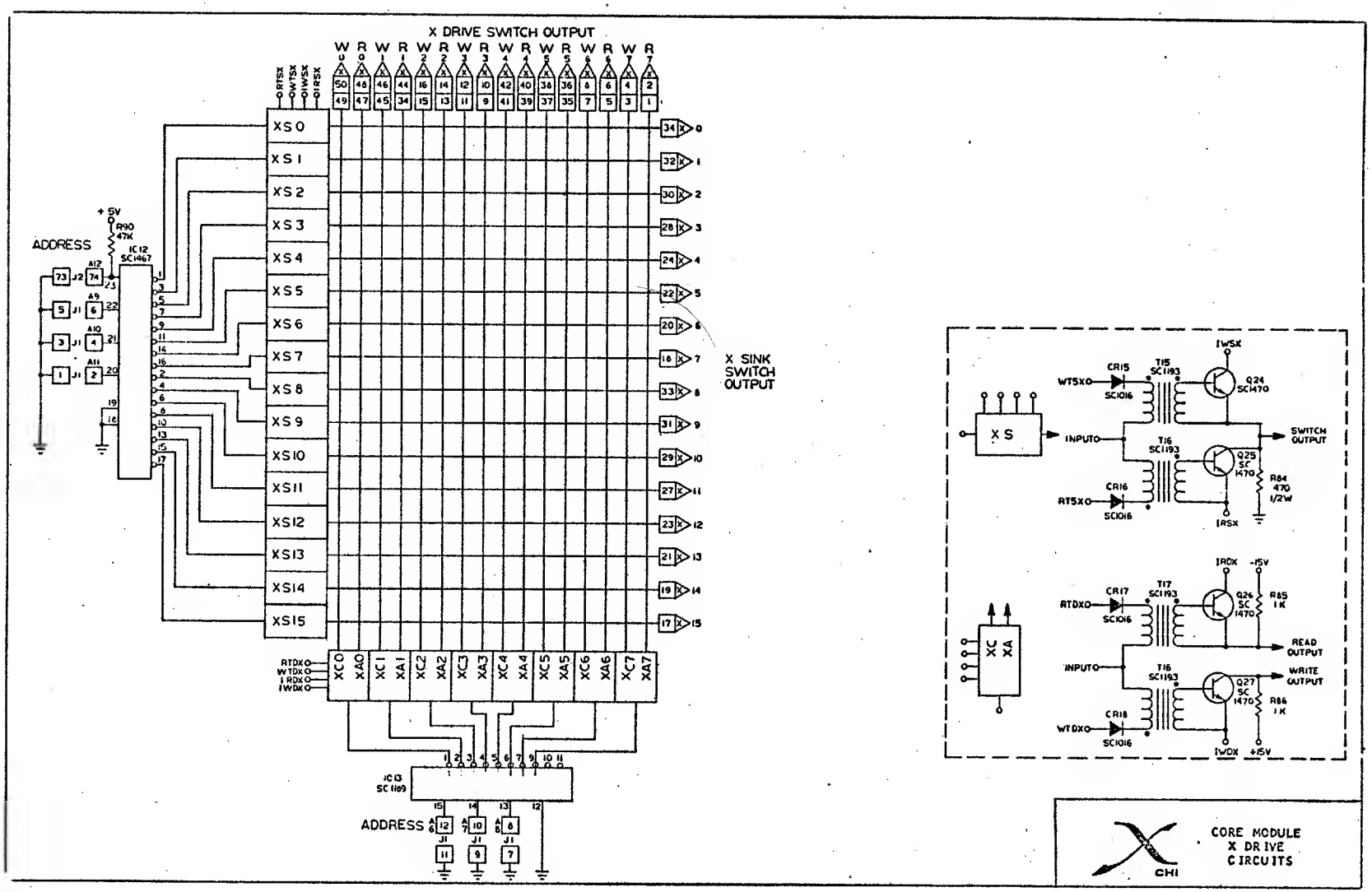

X DRIVE SWITCH OUTPUT
W R W R W R W R W R W R W R W R
0 0 1 1 2 2 3 3 4 4 5 5 6 6 7 7
RTSX
OWTSX
OWSX
OIRSX
XS0
XS1
XS2
XS3
XS4
XS5
XS6
XS7
XS8
XS9
XS10
XS11
XS12
XS13
XS14
XS15
X SINK SWITCH OUTPUT
+5V
R90 47K
ADDRESS
IC12 SC1467
IC13 SC1189
ADDRESS
RTDXO
WTDXO
IRDXO
IWDXO
XC0 XA0 XC1 XA1 XC2 XA2 XC3 XA3 XC4 XA4 XC5 XA5 XC6 XA6 XC7 XA7
IWSX
CR15
T15 SC1193
Q24 SC1470
WT5XO
SCI016
XS
INPUT0
SWITCH OUTPUT
T16 SC1193
Q25 SC 1470
R84 470 1/2W
CR16
RT5XO
IRSX
IRDX
-15V
CR17
T17 SC1193
Q26 SC 1470
R85 1K
RTDXO
READ OUTPUT
XC
XA
INPUT0
T18 SC1193
Q27 SC 1470
WRITE OUTPUT
R86 1K
CR18
WTDXO
IWDX
+15V
CHI
CORE MODULE
X DRIVE
CIRCUITS

FIGURE 13C

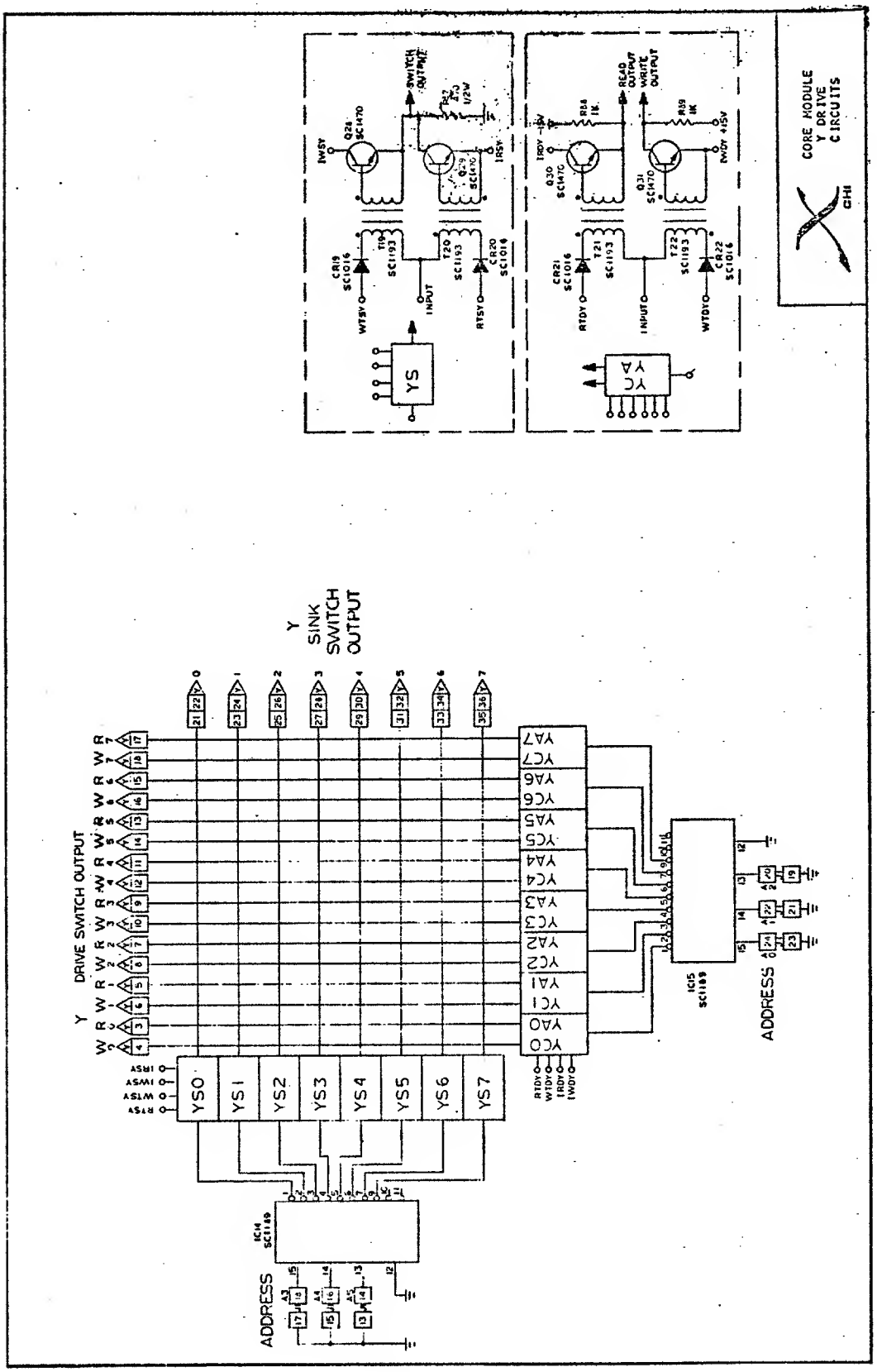

CORE MODULE
Y DRIVE
CIRCUITS
CHI
Y SINK SWITCH OUTPUT
Y DRIVE SWITCH OUTPUT
ADDRESS
YS0
YS1
YS2
YS3
YS4
YS5
YS6
YS7
YA0
YA1
YA2
YA3
YA4
YA5
YA6
YA7
YC0
YC1
YC2
YC3
YC4
YC5
YC6
YC7

FIGURE 13D

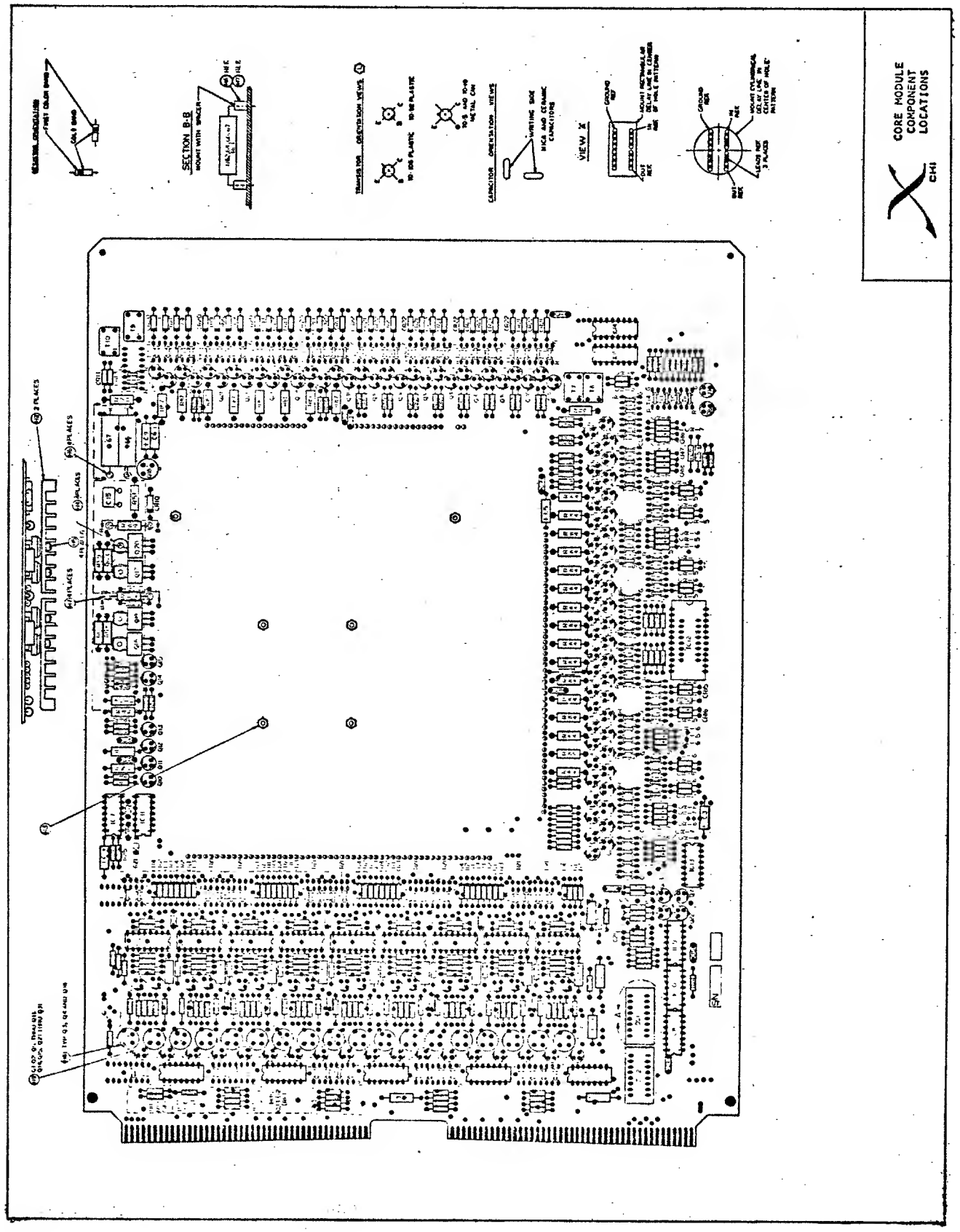
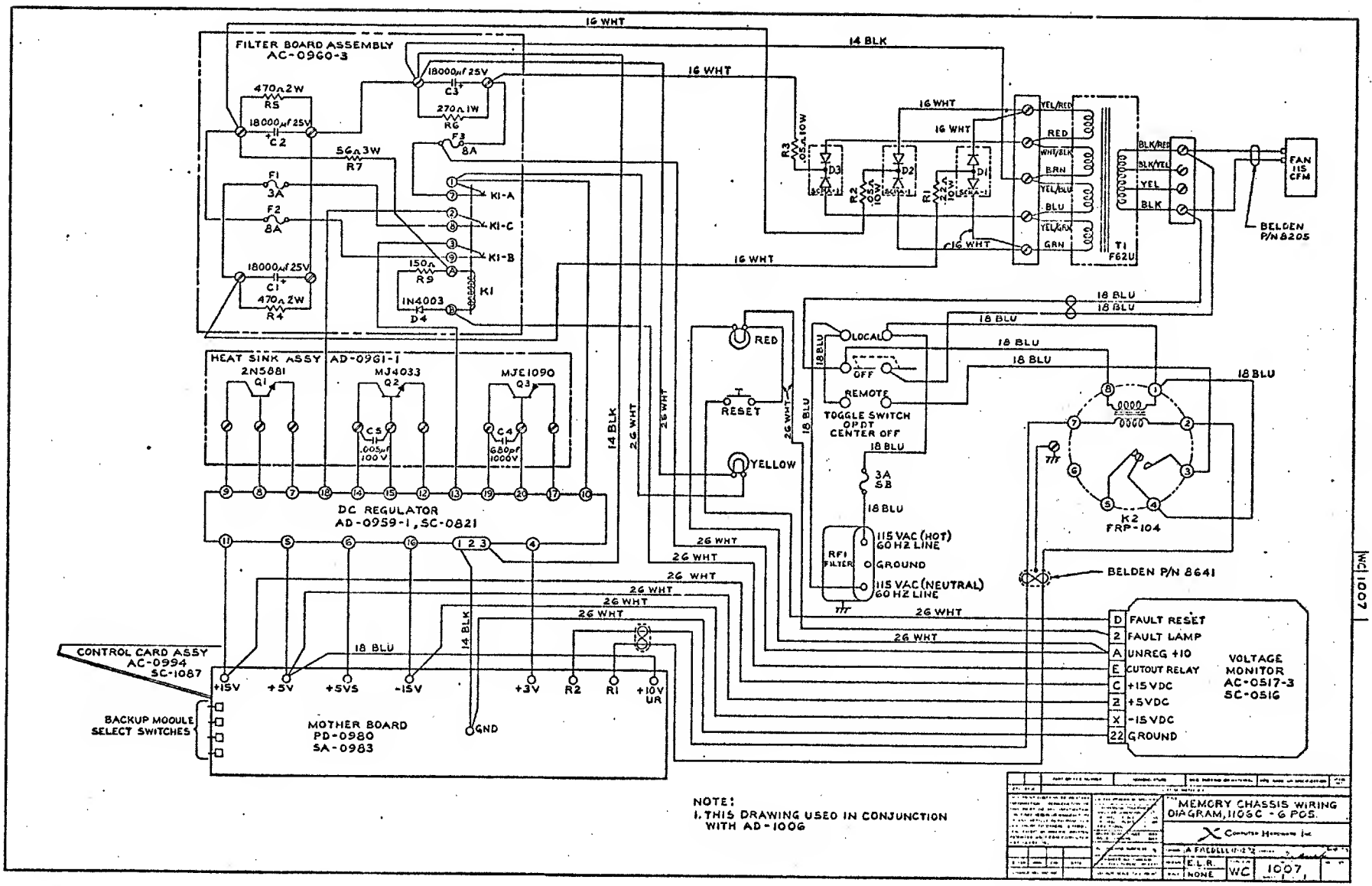


FIGURE 13E



NOTE:
1. THIS DRAWING USED IN CONJUNCTION WITH AD-1006

FIGURE 14A

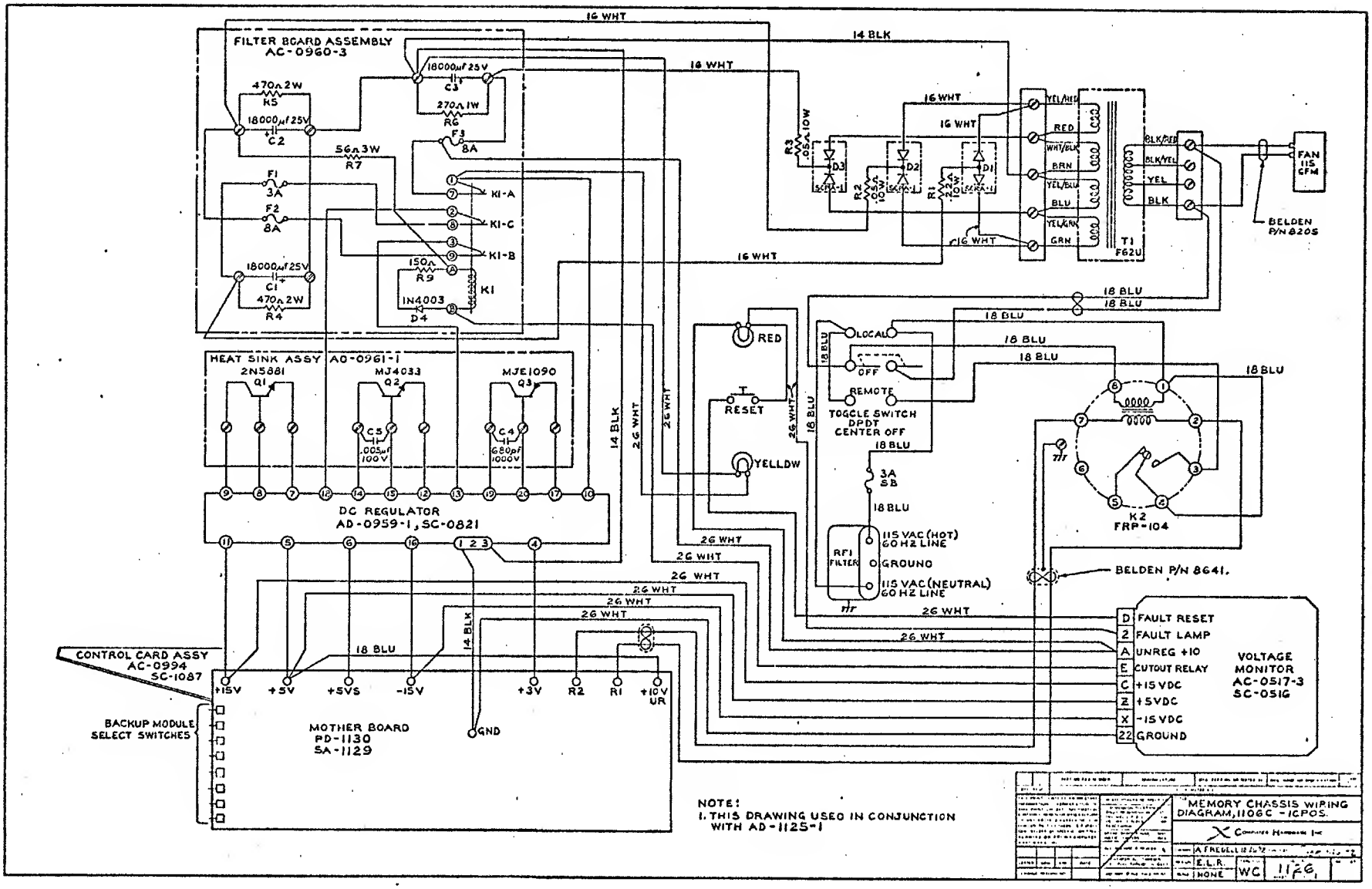
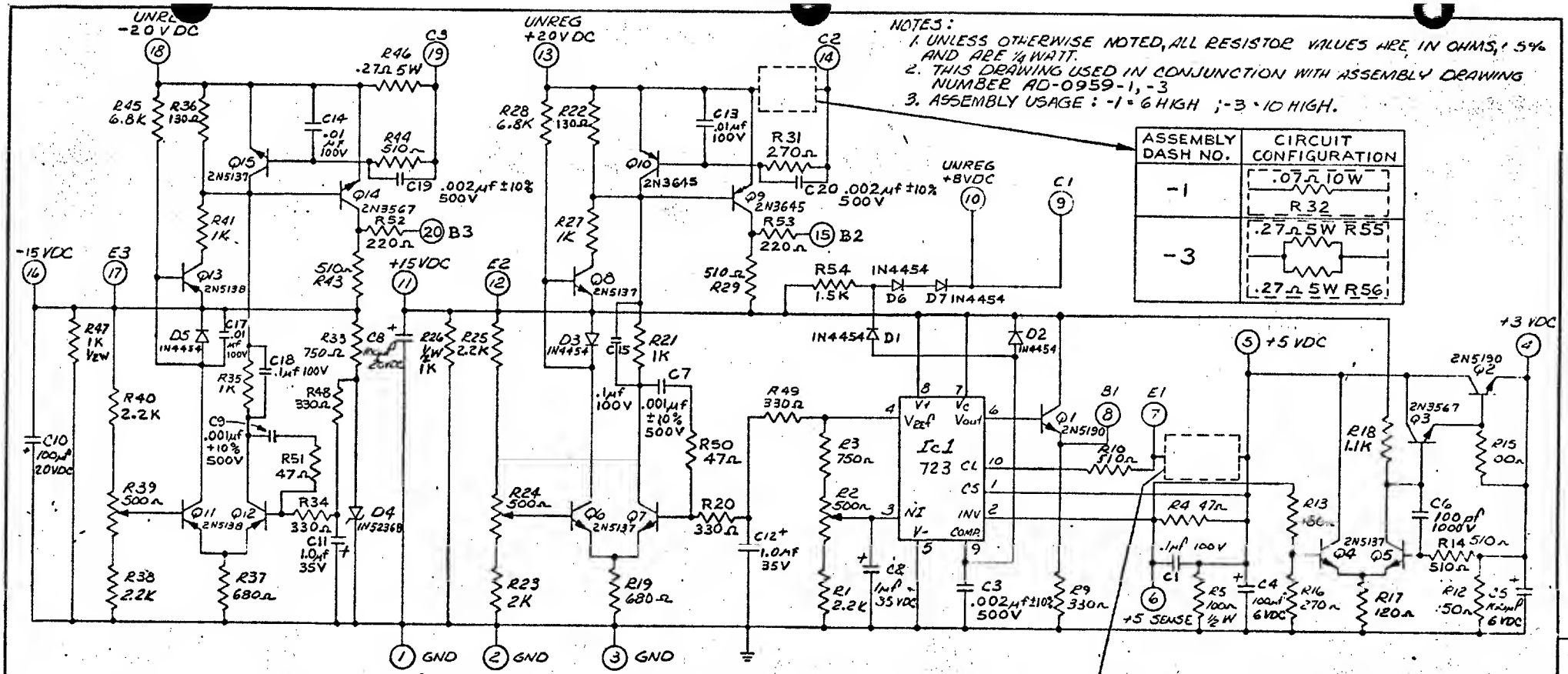

FILTER BOARD ASSEMBLY
AC-0960-3
HEAT SINK ASSY AO-0961-1
2N5881
MJ4033
MJE1090
DC REGULATOR
AD-0959-1, SC-0821
CONTROL CARD ASSY
AC-0994
SC-1087
BACKUP MODULE
SELECT SWITCHES
MOTHER BOARD
PD-1130
SA-1129
TOGGLE SWITCH
DPDT
CENTER OFF
LOCAL
OFF
REMOTE
RESET
RED
YELLOW
K1
K2
FRP-104
RFI FILTER
115 VAC (HOT) 60 HZ LINE
GROUND
115 VAC (NEUTRAL) 60 HZ LINE
BELDEN P/N 8641
BELDEN P/N 8205
FAN 115 CFM
T1 F62U
VOLTAGE MONITOR
AC-0517-3
SC-0516
D FAULT RESET
2 FAULT LAMP
A UNREG +10
E CUTOUT RELAY
C +15 VDC
Z +5 VDC
X -15 VDC
22 GROUND
16 WHT
14 BLK
18 WHT
18 BLU
26 WHT
NOTE:
1. THIS DRAWING USED IN CONJUNCTION WITH AD-1125-1
MEMORY CHASSIS WIRING DIAGRAM, 1106C - 16POS.
E.L.R.
WC 1126

FIGURE 14B



NOTES:
1. UNLESS OTHERWISE NOTED, ALL RESISTOR VALUES ARE IN OHMS, ± 5% AND ARE ½ WATT.
2. THIS DRAWING USED IN CONJUNCTION WITH ASSEMBLY DRAWING NUMBER AD-0959-1, -3
3. ASSEMBLY USAGE : -1 = 6 HIGH ; -3 = 10 HIGH.

ASSEMBLY DASH NO.	CIRCUIT CONFIGURATION
-1	.07Ω 10W R32
-3	.27Ω 5W R55 / .27Ω 5W R56

ASSEMBLY DASH NO.	CIRCUIT CONFIGURATION
-1	.07Ω 10W R11
-3	.27Ω 5W R57 / R11 / .07Ω 10W

17-10

FIG 15A

C.E. COPY

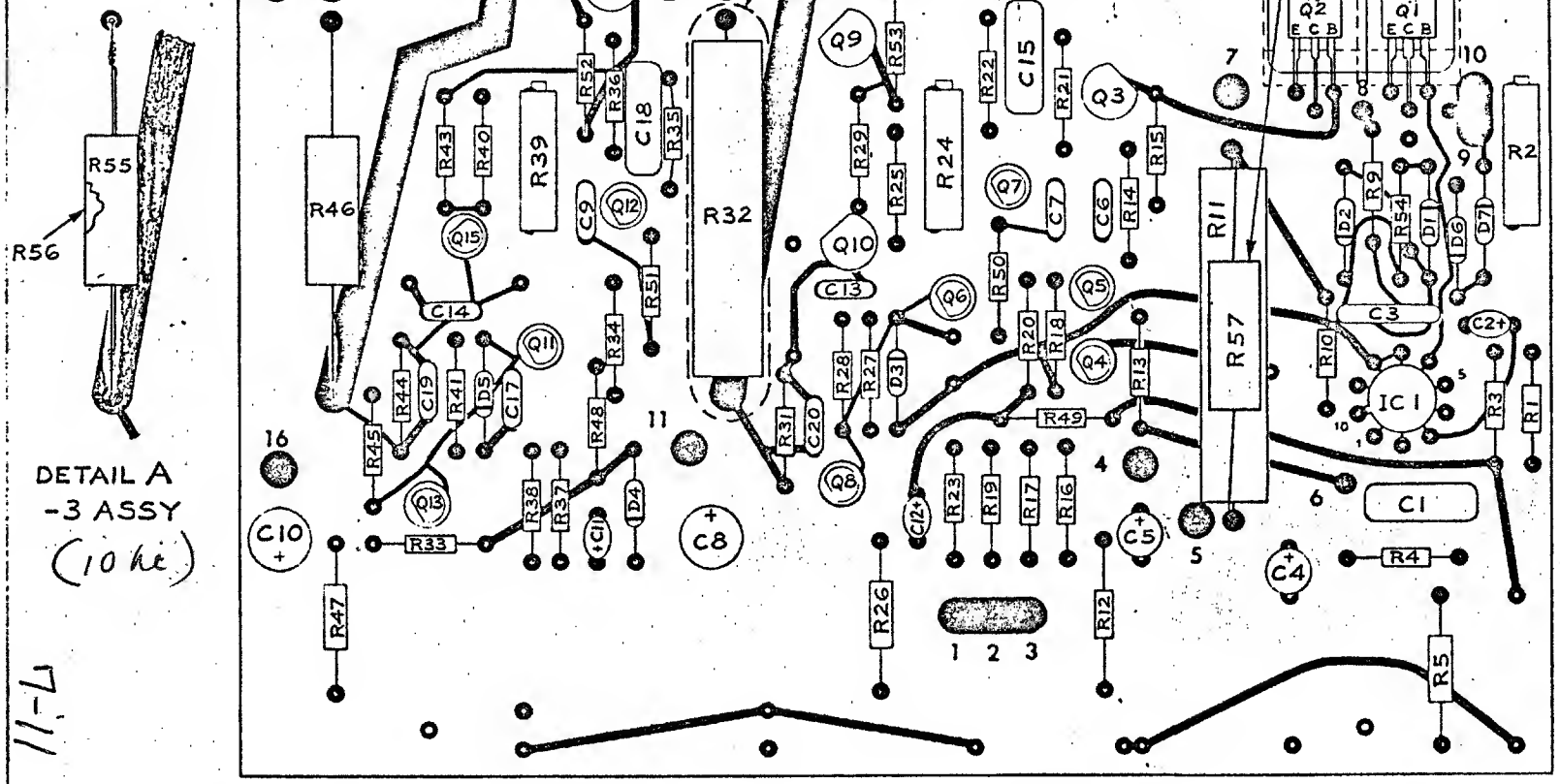
SC 0821

K	A.F		13-26-74
LETTER	DWN	CHK	DATE
			0821

REGULATOR, DC - 1106

X COMPUTER HARDWARE INC.

DRAWN	H. SANDERS	5/11/72	CHECK 6/25/72
DESIGN	HAL BROOK	SC	0821 K
SCALE	NONE		SHEET 1 OF 2



PART OR FILE NUMBER	NOMENCLATURE	MFG. PART NO. OR MATERIAL	MFG. NAME OR SPECIFICATION	ITEM NO.
QTY. REQD.	LIST OF MATERIALS			

THIS PRINT CONTAINS PROPRIETARY INFORMATION. REPRODUCTION OF THIS PRINT OR ANY INFORMATION CONTAINED HEREIN OR MANUFACTURE OF ANY ARTICLE HEREFROM, FOR DISCLOSURE TO OTHERS, IS FORBIDDEN, EXCEPT BY SPECIFIC WRITTEN PERMISSION FROM COMPUTER HARDWARE INC.

UNLESS OTHERWISE SPECIFIED
DIMENSION TOLERANCES
ANGULAR DIMENSION ±1/2°
DECIMAL 2 PLACE ± .010
DECIMAL 3 PLACE ± .005
FRACTIONAL ±
BREAK SHARP EDGES MAX.
INSIDE CORNERS MAX
ALL MACHINE SURFACES √
CHAMFER ALL THREADS 45° X FULL THREAD (INTERNT)
DO NOT SCALE THIS PRINT

TITLE: REGULATOR, DC-1106

X COMPUTER HARDWARE INC.

LETTER	DRN	CHK.	DATE
CHANGE RECORD NO.			0821

DRAWN: A. FREDELL
CHECKED: 10-16-72
DESIGN: HOLBROOK
TYPE-SIZE: SC
DWG. NO.: 0821 SHEET 2 OF 2
REV. LET.: J
SCALE:

SC 0821

7-11

F16-153

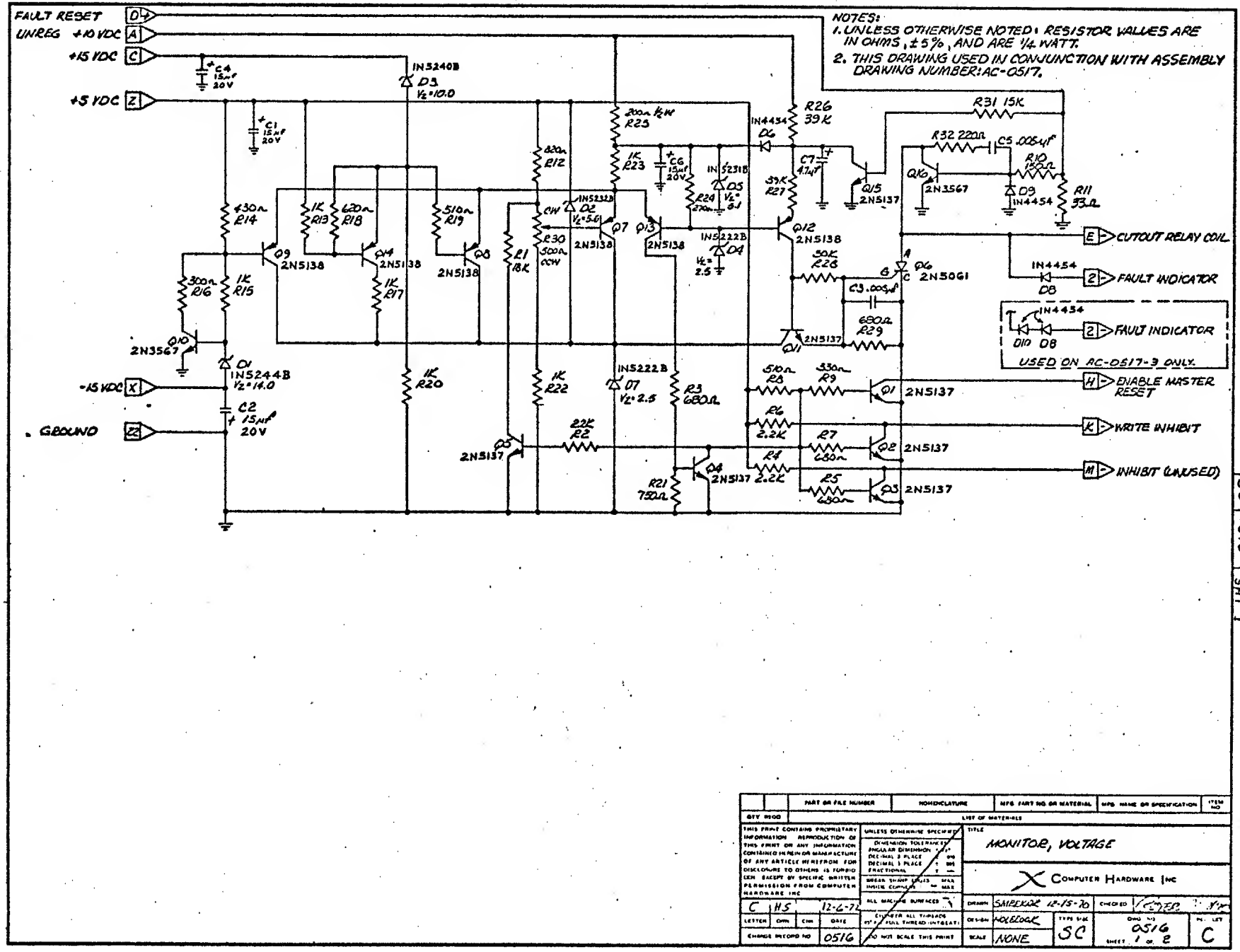

NOTES:
1. UNLESS OTHERWISE NOTED, RESISTOR VALUES ARE IN OHMS, ±5%, AND ARE ¼ WATT.
2. THIS DRAWING USED IN CONJUNCTION WITH ASSEMBLY DRAWING NUMBER: AC-0517.
FAULT RESET
UNREG +10 VDC
+15 VDC
+5 VDC
-15 VDC
GROUND
CUTOUT RELAY COIL
FAULT INDICATOR
FAULT INDICATOR
USED ON AC-0517-3 ONLY.
ENABLE MASTER RESET
WRITE INHIBIT
INHIBIT (UNUSED)
MONITOR, VOLTAGE
COMPUTER HARDWARE INC
SC 0516 SHT 1

FIGURE 16A

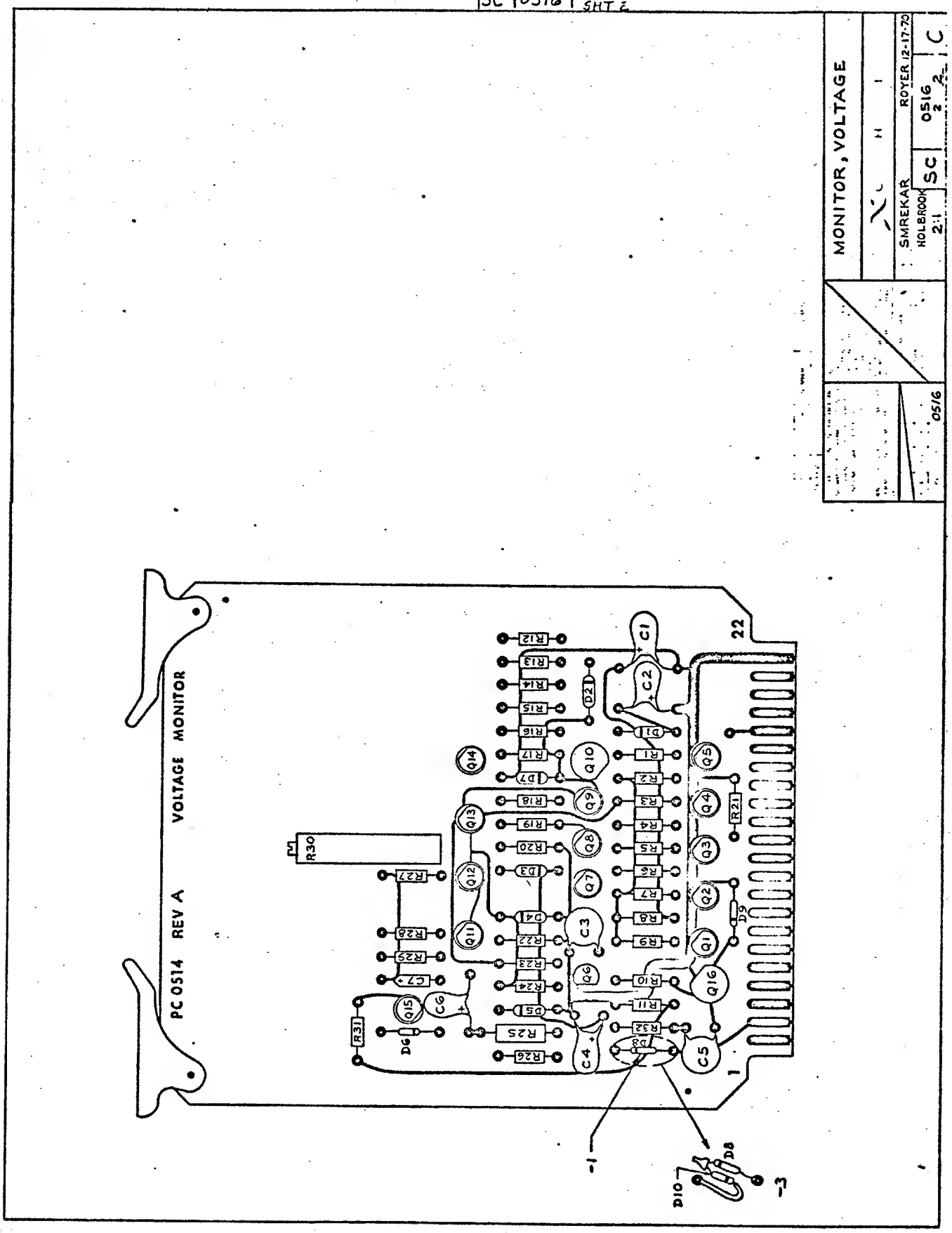

MONITOR, VOLTAGE
SMREKAR
HOLBROOK
2:1
SC
0516
2
ROYER 12-17-70
C
0516
PC 0514 REV A VOLTAGE MONITOR
22
1
-1
-3
D8
D10
R30
C1
C2
C3
C4
C5
C6
C7
D2
D1
D7
D3
D4
D5
D6
R21
R25
R31
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16

FIGURE 16B

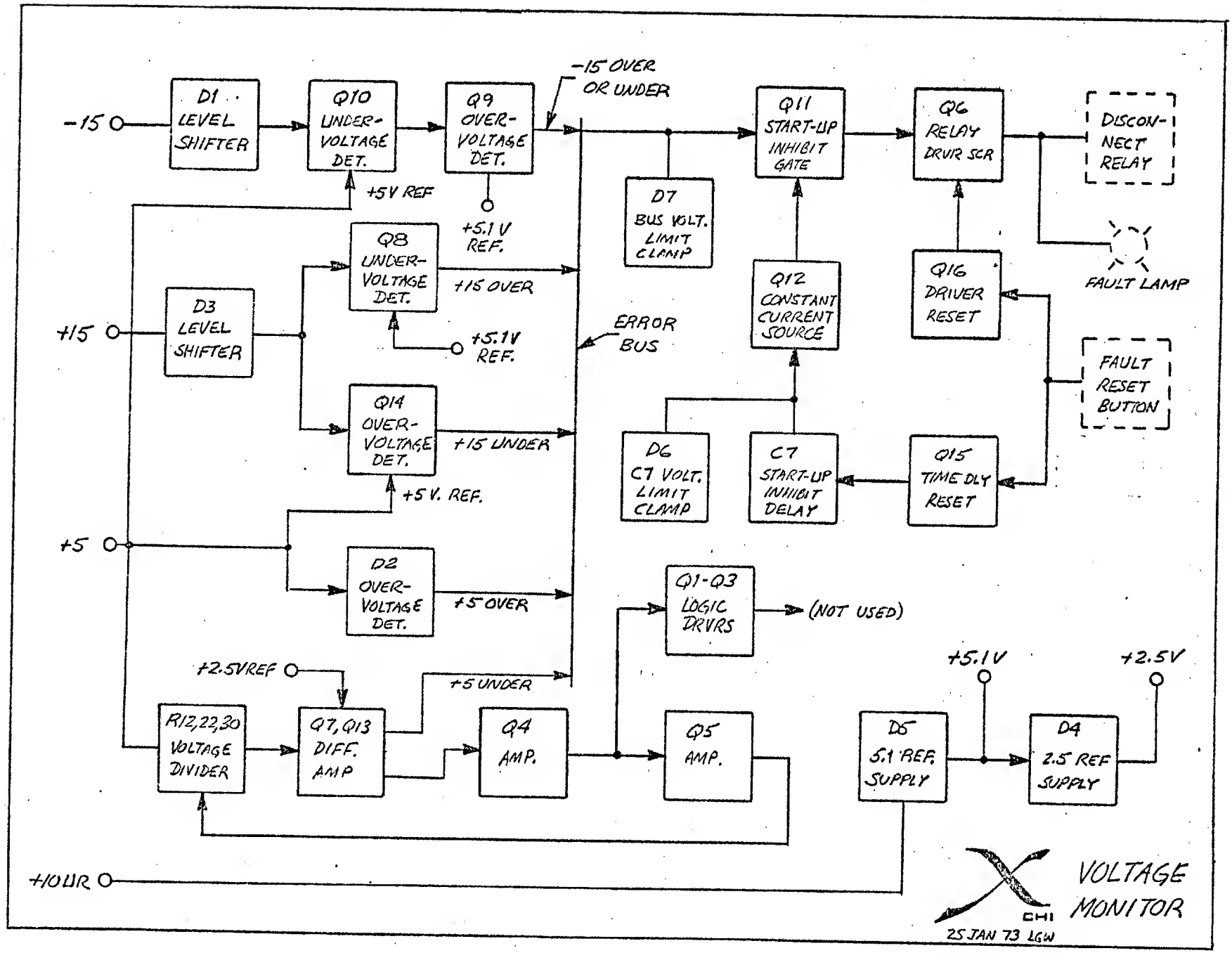

-15
D1 LEVEL SHIFTER
Q10 UNDER-VOLTAGE DET.
Q9 OVER-VOLTAGE DET.
-15 OVER OR UNDER
Q11 START-UP INHIBIT GATE
Q6 RELAY DRVR SCR
DISCON-NECT RELAY
+5V REF
+5.1 V REF.
D7 BUS VOLT. LIMIT CLAMP
FAULT LAMP
Q8 UNDER-VOLTAGE DET.
+15 OVER
Q12 CONSTANT CURRENT SOURCE
Q16 DRIVER RESET
+15
D3 LEVEL SHIFTER
+5.1V REF.
ERROR BUS
FAULT RESET BUTTON
Q14 OVER-VOLTAGE DET.
+15 UNDER
D6 C7 VOLT. LIMIT CLAMP
C7 START-UP INHIBIT DELAY
Q15 TIME DLY RESET
+5 V. REF.
+5
D2 OVER-VOLTAGE DET.
+5 OVER
Q1-Q3 LOGIC DRVRS
(NOT USED)
+2.5VREF
+5 UNDER
+5.1V
+2.5V
R12,22,30 VOLTAGE DIVIDER
Q7, Q13 DIFF. AMP
Q4 AMP.
Q5 AMP.
D5 5.1 REF. SUPPLY
D4 2.5 REF SUPPLY
+10UR
CHI
VOLTAGE MONITOR
25 JAN 73 LGW

FIGURE 17

TITLE

SIGNAL LIST
1106C CPU CABLE -1130

COMPUTER HARDWARE INC.

SIGNAL NAME	IBM DWG. REF	IBM PIN	CPU CONN. SIGNAL	CPU CONN. RTN.	R/D CONN. SIGNAL	R/D CONN. RTN
-STORAGE ADDRESS 3	MB111AA4	BB1 F2 D02 & BB1 F6 D02	BB1 T3+12" WITH 4" TAP	B1T3-13	J5B8 & J6B29	J6A29
4	MB111AB4	BB1 H1 B11	BB1 T3-6		J5B13	J5A17
5	MB111AC4	BB1 H1 B09	BB1 T3-5		J5B14	J5A17
6	MB111AD4	BB1 H1 C11	BB1 T3-8		J5B16	J5A18
7	MB111AE4	BB1 H1 C09	BB1 T3-7		J5B18	J5A18
8	MB111AF4	BB1 J1 C11	BB1 T3-18		J5B23	J5A27
9	MB111AG4	BB1 J1 C09	BB1 T3-17		J5B24	J5A27
10	MB111AH4	BB1 J1 D11	BB1 T3-20		J5B26	J5A28
11	MB111AJ4	BB1 J1 D09	BB1 T3-19		J5B28	J5A28
12	MB111AK4	BB1 J1 E11	BB1 T3-22		J6B1	J6A5
13	MB111AL4	BB1 J1 E09	BB1 T3-21		J6B2	J6A5
14	MB111AM4	BB1 K1 A11	BB1 T3-24		J6B4	J6A6
-STORAGE ADDRESS 15	MB111AN4	BB1 K1 A09	BB1 T3-23	B1T3-13	J6B6	J6A6
-B BIT 0	RB101BH6	BC1 B1 A09	BC1 T1-3	C1T1-13	J5B1	J5A7
1	RB111BH6	BC1 B1 B09	BC1 T1-5		J5B2	J5A8
2	RB121BH6	BC1 B1 C09	BC1 T1-7		J5B5	J5A8
3	RB131BH6	BC1 B1 D09	BC1 T1-9		J5B7	J5A9
4	RB141BH6	BC1 B1 E09	BC1 T1-11		J5B11	J5A16
5	RB151BH6	BC1 C1 B09	BC1 T1-15		J5B12	J5A16
6	RB161BH6	BC1 C1 C09	BC1 T1-17		J5B15	J5A17
7	RB171BH6	BC1 C1 D09	BC1 T1-19		J5B17	J5A18
-B BIT 8	RB201BH6	BC1 C1 E09	BC1 T1-21	C1T1-13	J5B21	J5A26

NOTES:
1. SINGLE WIRES FROM CPU CONNECTORS (PADDLE CARDS) ARE IDENTIFIED BY LENGTH, E.G. T4+5".
2. SEE 1106C TECHNICAL MANUAL, SECTION 2 FOR CONNECTION POINT.
3. REMOVED.
4. USED WITH PART NUMBER CD-1008-1.

TYPE-SIZE	DWG. NO.	REV LET
SA	1093 SHEET 1 OF 3	A1

FIGURE 18 A

TITLE

SIGNAL LIST
1106C CPU CABLE -1130

COMPUTER HARDWARE INC.

SIGNAL NAME	IBM DWG. REF	IBM PIN	CPU CONN.		R/D CONN.	
			SIGNAL	RTN.	SIGNAL	RTN
-S BIT 9	RB211BH6	BC1 D1 A09	BC1 T1-23	C1T1-13	J5B22	J5A26
10	RB221BH6	BB1 L1 A09	BB1 T4-3	B1T4-13	J5B25	J5A27
11	RB231BH6	BB1 L1 B09	BB1 T4-5		J5B27	J5A28
12	RB241BH6	BB1 L1 C09	BB1 T4-7		J5B29	J6A4
13	RB251BH6	BB1 L1 D09	BB1 T4-9		J5B30	J6A4
14	RB261BH6	BB1 L1 E09	BB1 T4-11		J6B3	J6A5
-B BIT 15	RB271BH6	BB1 M1 B09	BB1 T4-15	B1T4-13	J6B5	J6A6
-B BIT CK 1	KR111BE4	BB1 M1 C09	BB1 T4-17	B1T4-13	J6B7	J6A7
-B BIT CK 2	KR111BF4	BB1 M1 D09	BB1 T4-19	B1T4-13	J6B8	J6A8
-SENSE AMP BIT 0	RB101	BC1 B1 A11	BC1 T1-4	C1T1-13	J5A2	J5A6
1	RB111	BC1 B1 B11	BC1 T1-6		J5A3	J5A6
2	RB121	BC1 B1 C11	BC1 T1-8		J5A4	J5A7
3	RB131	BC1 B1 D11	BC1 T1-10		J5A5	J5A7
4	RB141	BC1 B1 E11	BC1 T1-12		J5A11	J5A15
5	RB151	BC1 C1 B11	BC1 T1-16		J5A12	J5A15
6	RB161	BC1 C1 C11	BC1 T1-18		J5A13	J5A15
7	RB171	BC1 C1 A11	BC1 T1-14		J5A14	J5A16
8	RB201	BC1 C1 E11	BC1 T1-22		J5A21	J5A25
9	RB211	BC1 D1 A11	BC1 T1-24	C1T1-13	J5A22	J5A25
10	RB221	BB1 L1 A09	BB1 T4-4	B1T4-13	J5A23	J5A25
11	RB231	BB1 L1 B09	BB1 T4-6		J5A24	J5A25
12	RB241	BB1 L1 C09	BB1 T4-8		J5A29	J6A3
-SENSE AMP BIT 13	RB251	BB1 L1 D09	BB1 T4-10	B1T4-13	J5A30	J6A3

TYPE-SIZE	DWG. NO.	REV. LET.
SA	1093 SHEET 2 OF 3	A1

FIGURE 18 B

TITLE

SIGNAL LIST
1106C CPU CABLE -1130

COMPUTER HARDWARE INC.

SIGNAL NAME	IBM DWG. REF	IBM PIN	CPU CONN. SIGNAL	CPU CONN. RTN.	R/D CONN. SIGNAL	R/D CONN. RTN
-SENSE AMP BIT 14	RB261	BB1 L1 E09	BB1 T4-12	B1T4-13	J6A1	J6A3
15	RB271	BB1 M1 B09	BB1 T4-16		J6A2	J6A4
16	KR111	BB1 M1 C09	BB1 T4-18		J6B9	J6A9
-SENSE AMP BIT 17	KR111	BB1 M1 D09	BB1 T4-14	B1T4-13	J6B10	J6A10
-CHAN ADDRESS BIT 0	FA131BB4	BB1 E6 B02	BB1 H6+4"	B1H6-13	J6B26	J6A26
-CHAN ADDRESS BIT 1	FA131BC4	BB1 H1 E09	BB1 T3-11	B1T3-13	J6B28	J6A28
-CHAN ADDRESS BIT 2	FA131BD4	BB1 J1 B09	BB1 T3-15	B1T3-13	J6B25	J6A25
+FILE ADDRESS BIT 1	XF231CC2	BB1 H6 D13	BB1 H6-23	B1H6-13	J6B15	J6A15
+FILE ADDRESS BIT 2	XF231BV2	BB1 H6 D09	BB1 H6-15	B1H6-13	J6B16	J6A16
+ M BIT 0	RB101	BB1 B3 B04	BB1 T4+8"	B1T3-13	J6B14	J6A14
+ M BIT 1	RB111BJ2	BB1 N4 B13	BB1 T4+5"	B1T4-13	J6B13	J6A13
+ M BIT 2	RB121BJ2	BB1 M2 B02	BB1 T3+4"	B1T3-13	J6B20	J6A20
- CS LEVEL 0	KM211AN4	BA1 B1 B09	BA1 T1-5	A1T1-13	J6B24	J6A24
- CS LEVELS	KM211BA4	BA1 B1 D09	BA1 T1-9	A1T1-13	J6B19	J6A19
-IX ADDR INHIBT SAR	KV301AT6	BA1 B1 E11	BA1 T1-12	A1T1-13	J6B18	J6A18
+STORAGE READ CYCLE	MC101AQ4	BB1 H1 E11	BB1 T3-12	B1T3-13	J6B12	J6A12
+STORAGE USE	MC101AW4	BB1 J1 B11	BB1 T3-16	B1T3-13	J6B27	J6A27
+STORAGE WRTE CYCLE	MC101AY4	BB1 G1 E11	BB1 T3-2	B1T3-13	J6B30	J6A30
CHI INHIBIT IBM		SEE NOTE 2	BC1 T1+8"	C1T1-13	J6B11	J6A11
+ 6V SENSE		BB1 H6 B11	BB1 H6-20	B1H6-13	J5A1	J5A6
+CE LAMP 3(M BIT 0)	ZL101	BA1 A4 B12	BA1 T1+8"	A1T1-13	J6B14	J6A14
+CE LAMP 1(READY)	ZL101	BA1 A3 B13	BA1 T1+6"		J5A20	

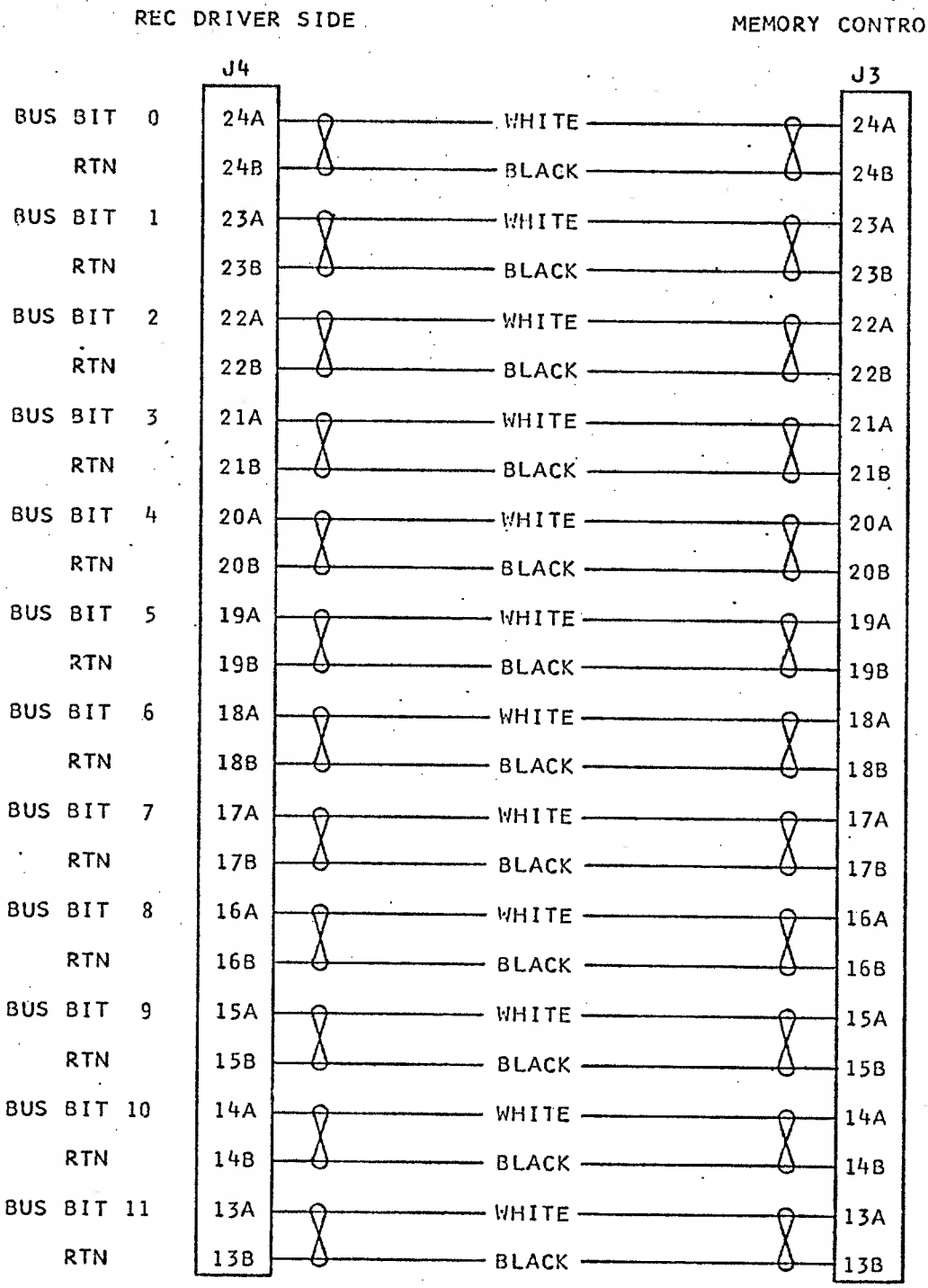
TYPE-SIZE	DWG. NO.	REV LET
SA	1093 SHEET 3 OF 3	A1

FIGURE 18 C

TITLE

1106C SIGNAL CABLE

COMPUTER HARDWARE INC.



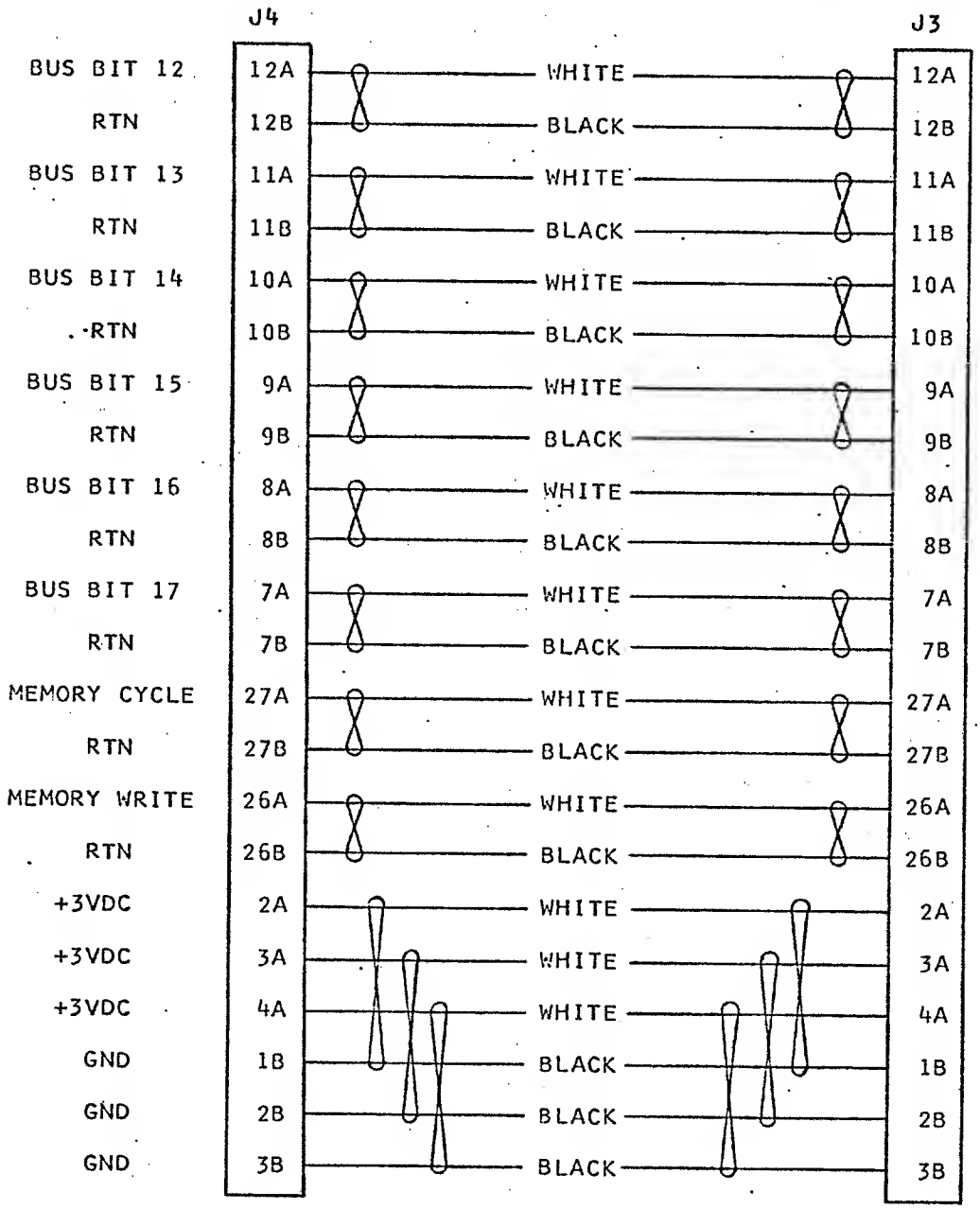
TYPE-SIZE	DWG. NO.	REV. LET.
WA	1223 SHEET 1 OF 3	NC1

FIGURE 19A

TITLE

1106C SIGNAL CABLE

COMPUTER HARDWARE INC.



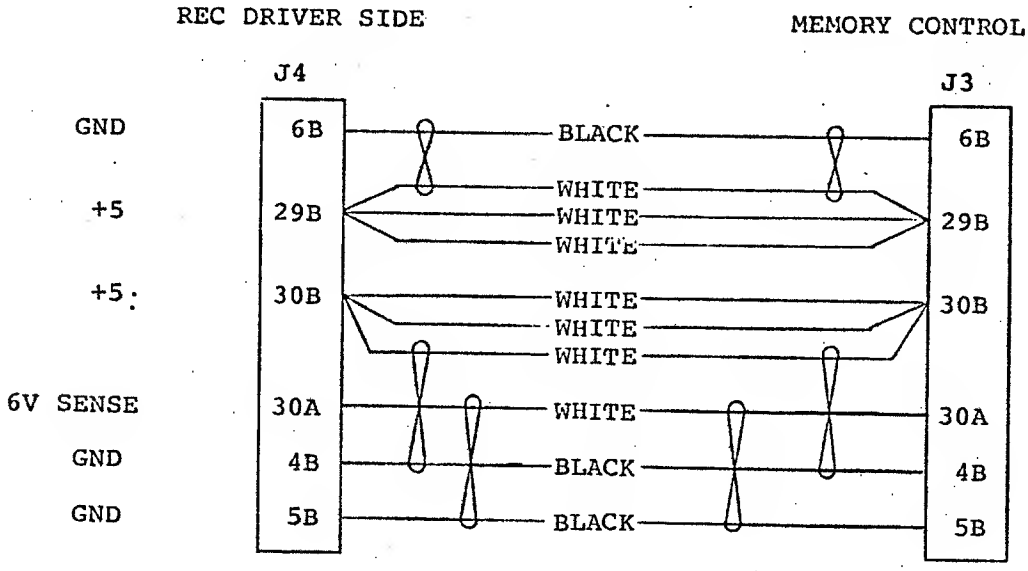
TYPE-SIZE	DWG. NO.	REV. LET.
WA	1223 SHEET 2 OF 3	NC1

FIGURE 19B

TITLE

1106 C SIGNAL CABLE

COMPUTER HARDWARE INC.



TYPE-SIZE	DWG NO.	REV. LET.
WA	1223 SHEET 3 OF 3	NC1

FIGURE 19C

Pin	Function	Pin	Function
1	Address, Bit 11 Return	2	Address, Bit 11
3	Address, Bit 10 Return	4	Address, Bit 10
5	Address, Bit 9 Return	6	Address, Bit 9
7	Address, Bit 8 Return	8	Address, Bit 8
9	Address, Bit 7 Return	10	Address, Bit 7
11	Address, Bit 6 Return	12	Address, Bit 6
13	Address, Bit 5 Return	14	Address, Bit 5
15	Address, Bit 4 Return	16	Address, Bit 4
17	Address, Bit 3 Return	18	Address, Bit 3
19	Address, Bit 2 Return	20	Address, Bit 2
21	Address, Bit 1 Return	22	Address, Bit 1
23	Address, Bit 0 Return	24	Address, Bit 0
25	Select B Return	26	Select B
27	Select B Return	28	Select B
29	Select B Return	30	Select B
31	Select B Return	32	Select B
33	Select A Return	34	Select A
35	Select A Return	36	Select A
37	Select A Return	38	Select A
39	Select A Return	40	Select A
41	Write Return	42	Write
43	Read Return	44	Read

CORE MODULE PIN ASSIGNMENTS (J1)

FIGURE 20A

Pin	Function	Pin	Function
45	Current Adjust Return	46	Current Adjust Test Point
47	Threshold Adjust Return	48	Threshold Adjust Test Point
49	Data Ready Return	50	Data Ready
51	Inhibit, Bit 1 Return	52	Inhibit, Bit 1
53	$\overline{CD}$ Bit 1 Return	54	$\overline{CD}$ Bit 1
55	$\overline{MD}$ Bit 1 Return	56	$\overline{MD}$ Bit 1
57	Inhibit, Bit 2 Return	58	Inhibit, Bit 2
59	$\overline{CD}$ Bit 2 Return	60	$\overline{CD}$ Bit 2
61	$\overline{MD}$ Bit 2 Return	62	$\overline{MD}$ Bit 2
63	Inhibit, Bit 3 Return	64	Inhibit, Bit 3
65	$\overline{CD}$ Bit 3 Return	66	$\overline{CD}$ Bit 3
67	$\overline{MD}$ Bit 3 Return	68	$\overline{MD}$ Bit 3
69	Inhibit, Bit 4 Return	70	Inhibit, Bit 4
71	$\overline{CD}$ Bit 4 Return	72	$\overline{CD}$ Bit 4
73	$\overline{MD}$ Bit 4 Return	74	$\overline{MD}$ Bit 4
75	Inhibit, Bit 5 Return	76	Inhibit, Bit 5
77	$\overline{CD}$ Bit 5 Return	78	$\overline{CD}$ Bit 5
79	$\overline{MD}$ Bit 5 Return	80	$\overline{MD}$ Bit 5
81	Inhibit, Bit 6 Return	82	Inhibit, Bit 6
83	$\overline{CD}$ Bit 6 Return	84	$\overline{CD}$ Bit 6
85	$\overline{MD}$ Bit 6 Return	86	$\overline{MD}$ Bit 6

CORE MODULE PIN ASSIGNMENTS (J1 CONT'D.)

FIGURE 20B

Pin	Function	Pin	Function
1	Inhibit, Bit 7 Return	2	Inhibit, Bit 7
3	$\overline{CD}$ Bit 7 Return	4	$\overline{CD}$ Bit 7
5	$\overline{MD}$ Bit 7 Return	6	$\overline{MD}$ Bit 7
7	Inhibit, Bit 8 Return	8	Inhibit, Bit 8
9	$\overline{CD}$ Bit 8 Return	10	$\overline{CD}$ Bit 8
11	$\overline{MD}$ Bit 8 Return	12	$\overline{MD}$ Bit 8
13	Inhibit, Bit 9 Return	14	Inhibit, Bit 9
15	$\overline{CD}$ Bit 9 Return	16	$\overline{CD}$ Bit 9
17	$\overline{MD}$ Bit 9 Return	18	$\overline{MD}$ Bit 9
19	Inhibit, Bit 10 Return	20	Inhibit, Bit 10
21	$\overline{CD}$ Bit 10 Return	22	$\overline{CD}$ Bit 10
23	$\overline{MD}$ Bit 10 Return	24	$\overline{MD}$ Bit 10
25	Inhibit, Bit 11 Return	26	Inhibit, Bit 11
27	$\overline{CD}$ Bit 11 Return	28	$\overline{CD}$ Bit 11
29	$\overline{MD}$ Bit 11 Return	30	$\overline{MD}$ Bit 11
31	Inhibit, Bit 12 Return	32	Inhibit, Bit 12
33	$\overline{CD}$ Bit 12 Return	34	$\overline{CD}$ Bit 12
35	$\overline{MD}$ Bit 12 Return	36	$\overline{MD}$ Bit 12
37	Inhibit, Bit 13 Return	38	Inhibit, Bit 13
39	$\overline{CD}$ Bit 13 Return	40	$\overline{CD}$ Bit 13
41	$\overline{MD}$ Bit 13 Return	42	$\overline{MD}$ Bit 13
43	Inhibit, Bit 14 Return	44	Inhibit, Bit 14

CORE MODULE PIN ASSIGNMENTS (J2)

FIGURE 20C

Pin	Function	Pin	Function
45	$\overline{CD}$ Bit 14 Return	46	$\overline{CD}$ Bit 14
47	$\overline{MD}$ Bit 14 Return	48	$\overline{MD}$ Bit 14
49	Inhibit, Bit 15 Return	50	Inhibit, Bit 15
51	$\overline{CD}$ Bit 15 Return	52	$\overline{CD}$ Bit 15
53	$\overline{MD}$ Bit 15 Return	54	$\overline{MD}$ Bit 15
55	Inhibit, Bit 16 Return	56	Inhibit, Bit 16
57	$\overline{CD}$ Bit 16 Return	58	$\overline{CD}$ Bit 16
59	$\overline{MD}$ Bit 16 Return	60	$\overline{MD}$ Bit 16
61	Inhibit, Bit 17 Return	62	Inhibit, Bit 17
63	$\overline{CD}$ Bit 17 Return	64	$\overline{CD}$ Bit 17
65	$\overline{MD}$ Bit 17 Return	66	$\overline{MD}$ Bit 17
67	Inhibit, Bit 18 Return	68	Inhibit, Bit 18
69	$\overline{CD}$ Bit 18 Return	70	$\overline{CD}$ Bit 18
71	$\overline{MD}$ Bit 18 Return	72	$\overline{MD}$ Bit 18
73	Address, Bit 12 Return	74	Address, Bit 12
75	$\overline{\text{Data Save}}$ Return	76	$\overline{\text{Data Save}}$
77	Not used	78	Not used
79	Ground	80	Ground
81	+5V	82	+5V
83	-15V	84	-15V
85	+15V	86	+15V

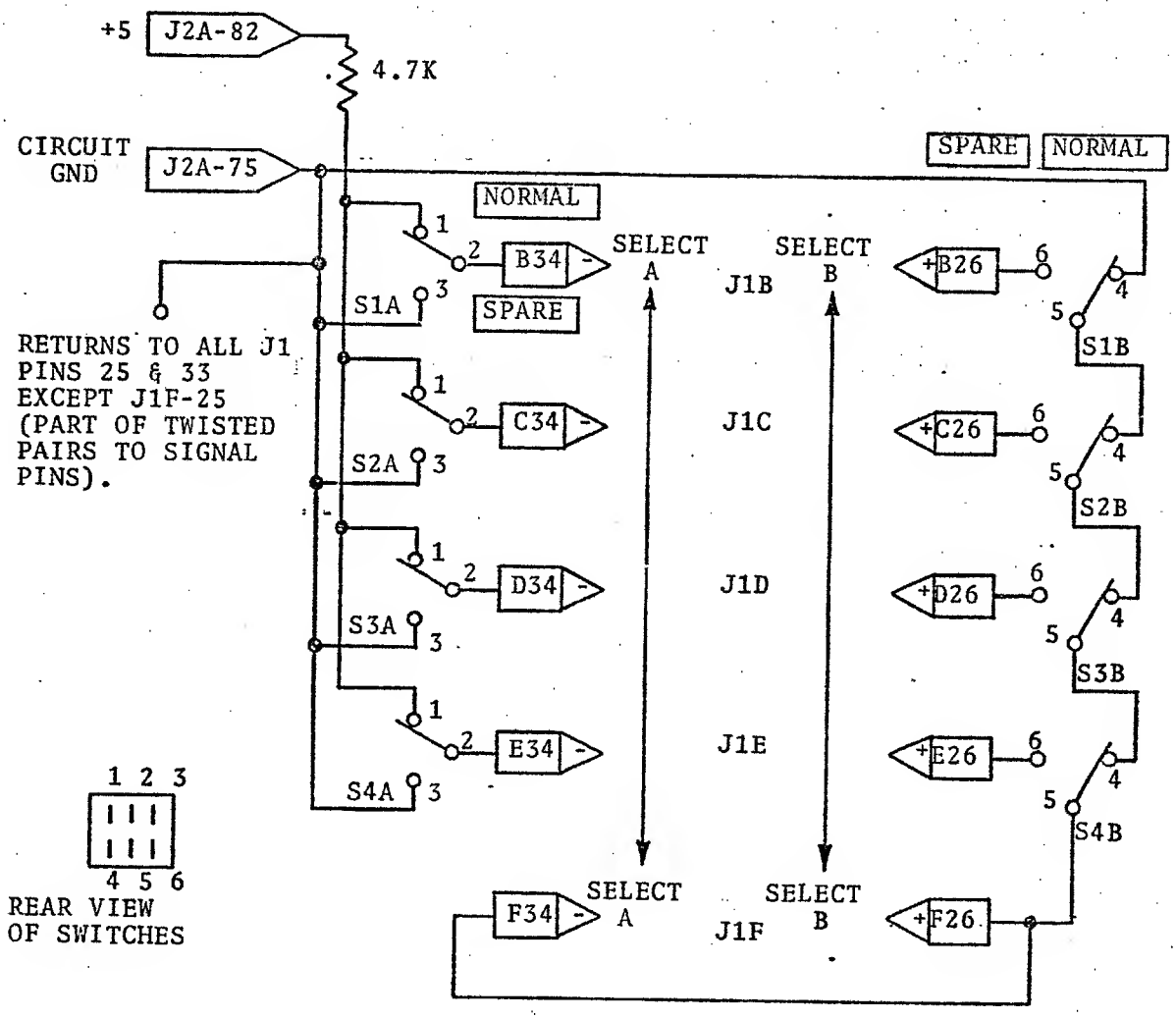
CORE MODULE PIN ASSIGNMENTS (J2 CONT'D.)

FIGURE 20D

TITLE

BACKUP MODULE SELECT SWITCHES
1106C 6 POSITION

COMPUTER HARDWARE INC.



NOTE:

1. EVEN NUMBERED PINS 26 THRU 32 AND 34 THRU 40 ARE DESIGNATED ON THE CORE MODULES AS "SELECT B", AND "SELECT A", RESPECTIVELY. THESE PINS ARE SHORTED WITHIN THE GROUPS WHEN A MODULE IS INSERTED.

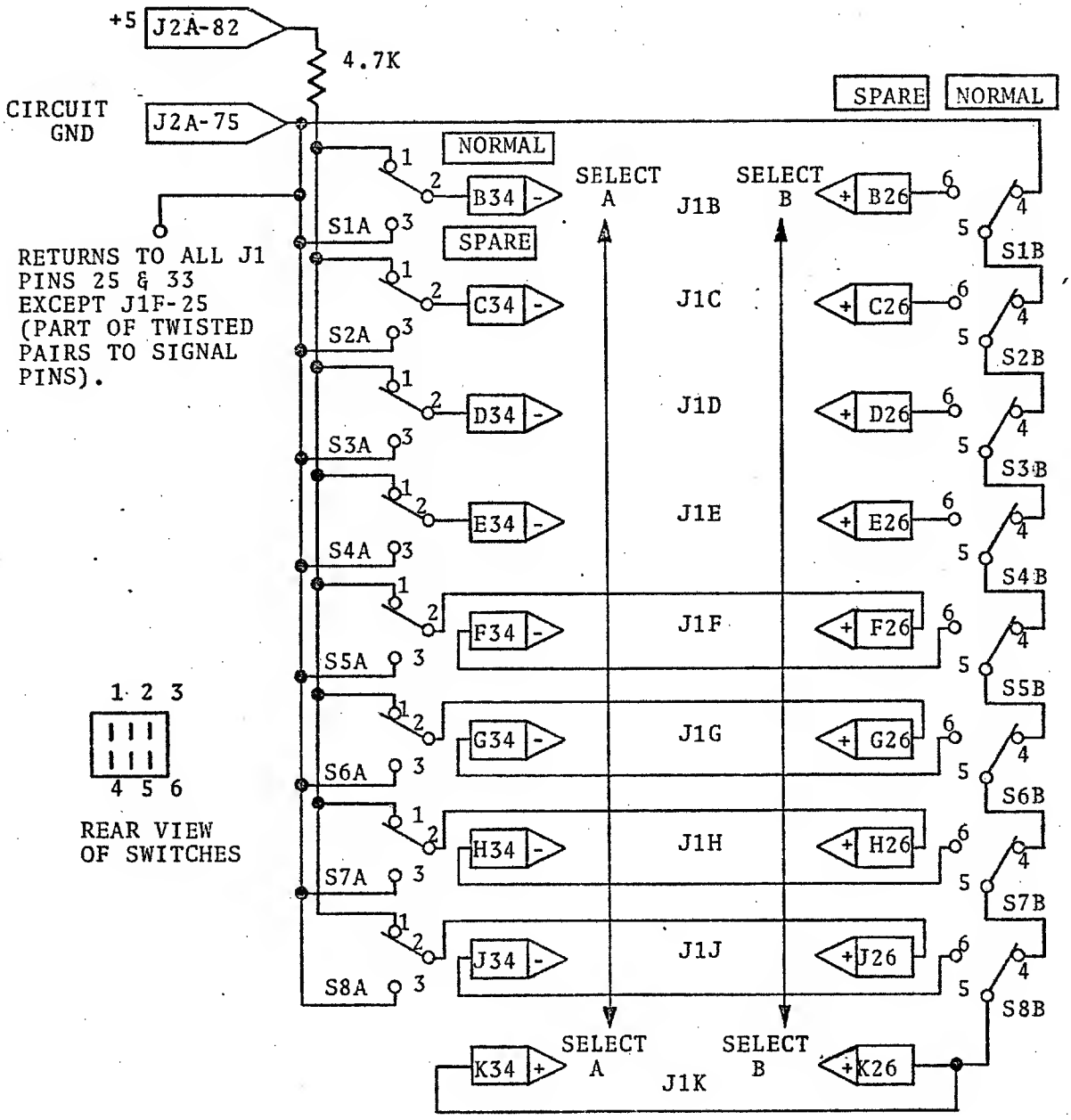
TYPE-SIZE	DWG. NO.	REV. LET.
SA	1283	
	SHEET 1 OF 1	

FIGURE 21A

TITLE

BACKUP MODULE SELECT SWITCHES
1106C 10 POSITION

COMPUTER HARDWARE INC.



NOTE:
1. EVEN NUMBERED PINS 26 THRU 32 AND 34 THRU 40 ARE DESIGNATED ON THE CORE MODULES AS "SELECT B", AND "SELECT A" RESPECTIVELY. THESE PINS ARE SHORTED WITHIN THE GROUPS WHEN A MODULE IS INSERTED.

TYPE-SIZE	DWG. NO.	REV. LET.
SA	1284 SHEET 1 OF 1	

FIGURE 21B

APPENDIX A

DIAGNOSTIC SOFTWARE

Core Function Test

The basic procedure to verify correct operation is to run the IBM HI Core Function Test (PID 03B0). This is loaded by use of the Relocatable Loader (PID 03AA).

Turn off all data switches and the CE PARITY RUN switch. Ready the reader with 03AA, 03B0 and one blank card and push RESET and PROGRAM LOAD. After reading all cards, the program will halt (B reg = 3001) showing the active address bits, ie. core size, in the accumulator. Press START to begin test; "BEGIN HI CORE TEST" will be printed on the console typer. Successful completion is indicated by a print out of "END HI CORE TEST".

Addressing errors will result in a print out and a wait (B reg = 3004) showing the bad data word in the accumulator and the correct word in the extension. Press START, and a second wait (B reg = 3005) will show the failed address in the accumulator. Parity errors will stop the CPU with the parity lamp lit and the failed address in the SAR. To get the waits and print out, START must be pushed with the C.E. PARITY RUN switch in the ON position. If no waits or print out is obtained, the parity bits themselves have failed rather than the data bits.

Detailed instructions may be located by consulting the index in the front of the first diagnostic manual (Machine type 1131, Volume A01).

40FF Test

This program fills each location of core with its own address plus one. If wrap-around occurs properly, it will halt at location 0000 because that location would now contain 0001 (0000+1). A wrap to another point will be similarly shown if the address is not the equivalent of an instruction which "blows" the program. The program can also be used to determine the location from which an improperly addressed read occurs, because it effectively labels each location in core.

(1) Load storage with 40FF.

(2) Push STOP and restore STORAGE LOAD switch.

(3) Push RESET and START.

Hi-Lo Test

This routine switches alternately between IBM and CHI core, starting at either depending on the version used.

(1) Load the program version selected via the data switches.

(2) Load IAR with the address of the first instruction.

(3) Push START.

Hi-Lo-Hi-Lo Version:

ADDRESS	CONTENTS
H	C400
H+1	L
H+2	4C00
H+3	H

Lo-Hi-Lo-Hi Version:

ADDRESS	CONTENTS
L	C400
L+1	H
L+2	4C00
L+3	L

Note: "H" is some high core location and "L" is some low core location.